Nonlinear Source Emulator

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DEDICATION

To my beloved parents

for their unending support and unconditional love

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and to my country that continues to give me the power to strive.

Abstract

The world is rapidly changing from using the fossil based energy, which is facing exhaustion and having a lot of environmental issues, to the use of renewable energy sources such as sun energy and wind energy. Energy from the sun has become an important source for terrestrial applications and remains the prime source of energy in non-terrestrial applications such as those in sky-explorers. However, a renewable energy source is expensive, bulky, and its performance is weather dependent, which make testing of downstream converters very difficult. As a result, a nonlinear source emulator (NSE) is a good solution to solve the problems associated with the use of real nonlinear sources in testing phases.

However, a recent technical survey conducted during this work shows that most existing NSEs have only been concerned with simulating nonlinear systems in terrestrial applications. Furthermore, their dynamic performance were not fast enough in order to imitate how a real nonlinear energy source would react under extreme conditions and operation modes. Particularly, a PV system in the sky can experience a step change of sunlight irradiation. Moreover, operation modes may include load step between nominal and open circuit, and load step between nominal and short circuit. Under these conditions, a practical nonlinear source system will react almost instantly, whereas the fastest among existing NSEs had a transient of about 3 milliseconds.

It is the highlight of this thesis, to demonstrate the development of a proposed NSE system with high dynamic performance. The goal of the work is to achieve a state-of-the art transient time of 10 μs. In order to produce the arbitrary nonlinear curve, the exponential function of a typical diode is used, but the diode can be replaced by other nonlinear curve reference generator unit.

Because nonlinear energy sources come in different sizes and power rating, a single NSE may not be sufficient to simulate a wide selection of nonlinear sources. For this reason, the proposed NSE system is realized as modules. Stacking or connecting multiple modules in parallel will allow simulation of nonlinear source systems with higher output power.

In this work, a module will consist of two fundamental units: an isolated power supply and an NSE. The isolated power supply has to possess a very low circuit input-to-output capacitance (very low C_{io}) in order to reduce the effect of conductive common-mode current produced by the high rate of change of voltage over time (high dv/dt) at the NSE output.

The contributions of the thesis are based on the development of both units: the low C_{io} isolated power supply and the high dynamic performance NSE. Both units are investigated theoretically and experimentally.

For the very low C_{io} power supply, we propose a new topology and control, together with a novel transformer structure, in which, its two windings are separated by a significant distance, in order to attain a low interwinding capacitance. A mathematical model is proposed to accurately model the interwinding capacitance of the proposed transformer. The result achieved is a total converter C_{io} of 10 pF in a 300-W prototype, which is 30 times lower than that of existing approaches.

For the NSE, we propose a new circuit consists of an ultrafast tracking converter and a novel nonlinear curve reference generator based on diode curve. Even though the nonlinear curve is based on diode p-n junction, the proposed NSE can simulate other arbitrary nonlinear sources if the diode is replaced by other appropriate nonlinear curve reference generator units. The prototype is 200-W rating. The experimental results show that the proposed NSE can react to a fast change in input source (such as an abrupt change of wind speed for wind turbine emulator), as well as to a load step from nominal to open circuit and vice versa, all within 10 μs.

The proposed NSE, therefore, offers the state-of-the-art dynamic performance among devices of the same kind. It also offers a complete solution for simulation of nonlinear source systems of different sizes, both in terrestrial and non-terrestrial applications.

Key words: **Current transformers, dc-dc power converters, hysteresis, parasitic capacitance,** PV **system, stacking, switching converters.**

Resumé

Verden er under hastig forandring fra at bruge fossilt baseret energi, som snart slipper op og har en masse miljøspørgsmål, til anvendelse af vedvarende energikilder såsom sol- og vindenergi. Energi fra solen er blevet en vigtig energikilde til jordbaserede anvendelser og er stadig den vigtigste kilde af energi til ikke-jordbaserede anvendelser, som f.eks. til udforskning af rummet. Men vedvarende energikilder er dyre, pladskrævende, og deres energiproduktion er afhængig af bl.a. vejret, klokken og årstiden. Dette gør test af de efterfølgende elektroniske omformere vanskelig. Som et resultat heraf vil en ulineær-kilde-emulator (NSE) være en god løsning til at løse de problemer, der er forbundet med brug af reelle ulineære energikilder i testfaserne.

Gennemgangen af kendte teknologier og teknikker i denne afhandling viser imidlertid, at de fleste eksisterende NSE'ere kun fokuserer på at simulere ulineære energikilder til jordbaserede applikationer. Desuden er deres dynamiske ydeevne ikke var hurtig nok til at efterligne, hvordan et rigtigt ulineær-kilde-system vil reagere under de ekstreme forhold og driftstilstande. Især et PV-system i rummet kan opleve et brat spring i solindstråling under en passage fra fuld sollys til fuldstændig skygge. Ved anvendelser benyttes ofte paralleltype ind- og udkobling eller serietype ind- og udkobling af belastningen eller batteriet, hvor ulineær-energikilden skifter hhv. fra kortslutning til fuld belastning eller fra åbent kredsløb til fuld belastning. Under disse betingelser vil et ulineær-kilde-system vil reagere indenfor omkring 10 mikrosekunder, mens de hurtigste blandt eksisterende NSE har en reaktionstid på cirka 3 millisekunder, dvs. 300 gange langsommere.

Kernen i denne afhandling er, at det er vist, at man kan lave en NSE med høj dynamisk ydeevne. Målet med dette arbejde er opnået med en reaktionstid på 10 mikrosekunder. For at kunne producere en vilkårlig ulineær kurve er eksponentialfunktionen fra en typisk diode blevet brugt, men dioden kan erstattes af andre ulineære kurve referenceenheder.

Fordi ulineær-kilde-systemer kommer i forskellige størrelser og effekter, vil en enkelt NSE måske ikke være tilstrækkelig til at simulere et bredt udvalg af ulineære energikilder. Af denne grund kan det foreslåede NSE-system realiseres som moduler. Serie- og parallelkobling af flere moduler vil muliggøre simulering af ulineær-kilde-systemer med højere udgangseffekt.

I dette arbejde består et modul af to grundlæggende enheder: En højisoleret strømforsyning og en NSE. Den højisolerede strømforsyning har en ekstremt lav kapacitet

mellem ind- og udgangen (meget lav Cio) med henblik på at reducere virkningen fra kapacitive common-mode strømme genereret af den høje ændringshastighed af spændingen per tid (høj dv/dt) på NSE'ens udgang.

De forskningsmæssige bidrag i denne afhandling er på forskningsresultaterne fra begge enheder: Den høj-isolerede strømforsyning og NSE'en med den høje dynamiske ydeevne. Begge enheder er undersøgt både teoretisk og eksperimentelt.

For den højisolerede strømforsyning, foreslås ny topologi og kontrol sammen med en ny transformerstruktur, som er de to viklinger adskilt af en betydelig afstand for at opnå en lav koblingskapacitet. En matematisk model modellerer koblingskapaciteten af foreslåede transformer. Det opnåede resultat er en samlet Cio på 10 pF for en 300 W prototype, det vil sige 30 gange lavere end for eksisterende fremgangsmåder.

For NSE'en foreslås et nyt kredsløb består af en ultrahurtig sporingskonverter og en ny ulineær-kilde-småsignalgenerator. Prototypen er på 200 W. De eksperimentelle resultater viser, at den foreslåede NSE kan reagere på ændringer indenfor 10 mikrosekunder.

Den foreslåede NSE har en overlegen dynamisk ydeevne sammenlignet med andre tilsvarende løsninger. Den giver også en komplet løsning til simulering af ulienærkilde-systemer i forskellige størrelser både til jordbaserede og ikke-jordbaserede anvendelser.

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Chapter 1

Introduction

1.1 Scope of the thesis

This thesis presents the results achieved from my Ph.D. project which was carried out at the Electronics Group, Department of Electrical Engineering, the Technical University of Denmark, during the period from December 01, 2011 to November 30, 2014. Most of the results have been documented and either published or submitted in forms of peer-reviewed conference or journal articles. Since the detail of the work can be found in the completed articles, which are included in Appendix A.1.–A.7. of the thesis, they are not going to be restated. Instead, the thesis aims at providing an overview of the problems studied and highlights of the solutions proposed. The detail, whenever needed, will mainly refer to the specific section of the published article for its description or discussion. The methods are discussed from a system level point of view. The key verification results are selected to demonstrate the effectiveness of the proposed solutions. Finally, the thesis will also provide supplement analysis and results in order to clarify or provide more insights into the problems studied.

A list of publications can be found in the back of the thesis prior to the appendix.

1.2 Background and Motivation

Nowadays, the majority of the current energy in the world is still produced by fossils (such as coal, oil, and natural gas) and nuclear fuels. However, the former source suffers from facing exhaustion due to limited available resources, and the latter suffers from safety problem, which can threaten the life of a large area surrounding. In addition to that, fossil fuels cause environmental pollution, which directly worsens the global warming problem. Furthermore, nuclear power plant by-product remains radioactive for thousands of years, which is harmful for society. For these reasons, there is a rapid move world wide, towards renewable energy systems.

Renewable energy systems such as those based on wind and sun energy are advanc-

ing rapidly both in volume, scale and in popularity. In testing and the development of the downstream power circuits based on renewable energy, such as maximum power point trackers (MPPTs) or energy storage elements, many tests have to be performed where the renewable energy sources have to undergo different environmental setting conditions. For example, the output of a wind turbine changes rapidly with wind speed and the direction of the wind, whereas a sun energy based system's output depends strongly on the sun irradiation, the air-mass (i.e., angular of the sunlight) and ambient temperature. All of these make the testing of renewable energy based subsystems very difficult. Furthermore, the cost and the size of a real renewable energy source to be used in tests can be very large. As a result, an alternative solution has been sought, which replaces the use of real renewable energy sources in ground testing by their hardware simulators. From the perspective of electrical engineering, a hardware simulator is a system based on electric circuits that can resemble the electrical characteristic of the object being simulated. It can be generalized by the name "nonlinear source emulator", i.e., "NSE" in abbreviation form.

Sun energy has been recently expanding its impact on terrestrial applications. For example, sun energy based systems can be found on the roof-tops of civil architecture, on street lights, cruise ships, etc. However, it should be noted that sun energy has been used much earlier in non-terrestrial applications. Sun energy has been the only power source that supplies energy to sky explorers. The conditions of the load connected with a nonlinear source system in general is unknown and can take many forms. It is highly desired that an NSE has a dynamic response which is as fast as possible in order to make it suitable for connecting with different unknown loads and unknown working conditions. The unknown load can be a maximum power point tracker (MPPT), or a load that is constantly switching both ways between nominal and open circuit, or between nominal and short circuit.

Researchers have proposed different NSEs. But to the best of the authors' knowledge, visibly reported works could have been made stackable in order to adapt to different power rating requests and made faster in terms of transient response in order to achieve better output power regulation.

It is the motivation of this project to develop a high dynamic performance NSE that addresses the aforementioned problems.

1.3 Thesis structure

The structure and contents of the thesis are graphically presented in Fig. 1.1. The structure is as follows. Chapter 1 clarifies the scope of the thesis, background and motivation, and describes the thesis structure. Chapter 2 reviews the state-of-the-art where existing solutions are assessed. Chapter 2 also discusses the proposed approach from a system level point of view. It also states the requirements for each subsystem of the proposed approach. Chapter 3 describes the modelling and design of the first subsystem, namely the ultra low circuit input-to-output capacitance power supply, which is intended to supply energy to the proposed NSE. Chapter 4 discusses recent finding during the development of a high dynamic performance NSE. Chapter 5 summarizes the work and discusses possible future work. The

complete bibliography is presented after the last chapter. Following that, a list of publications is provided. Finally, at the end of the thesis lies Appendix A. where all complete papers (A.1. to A.7.) resulting from this work are attached.

It is restated here, that the purpose of this dissertation is solely to summarize and supplement the already published papers by providing a coherent presentation of the overall project and related results.

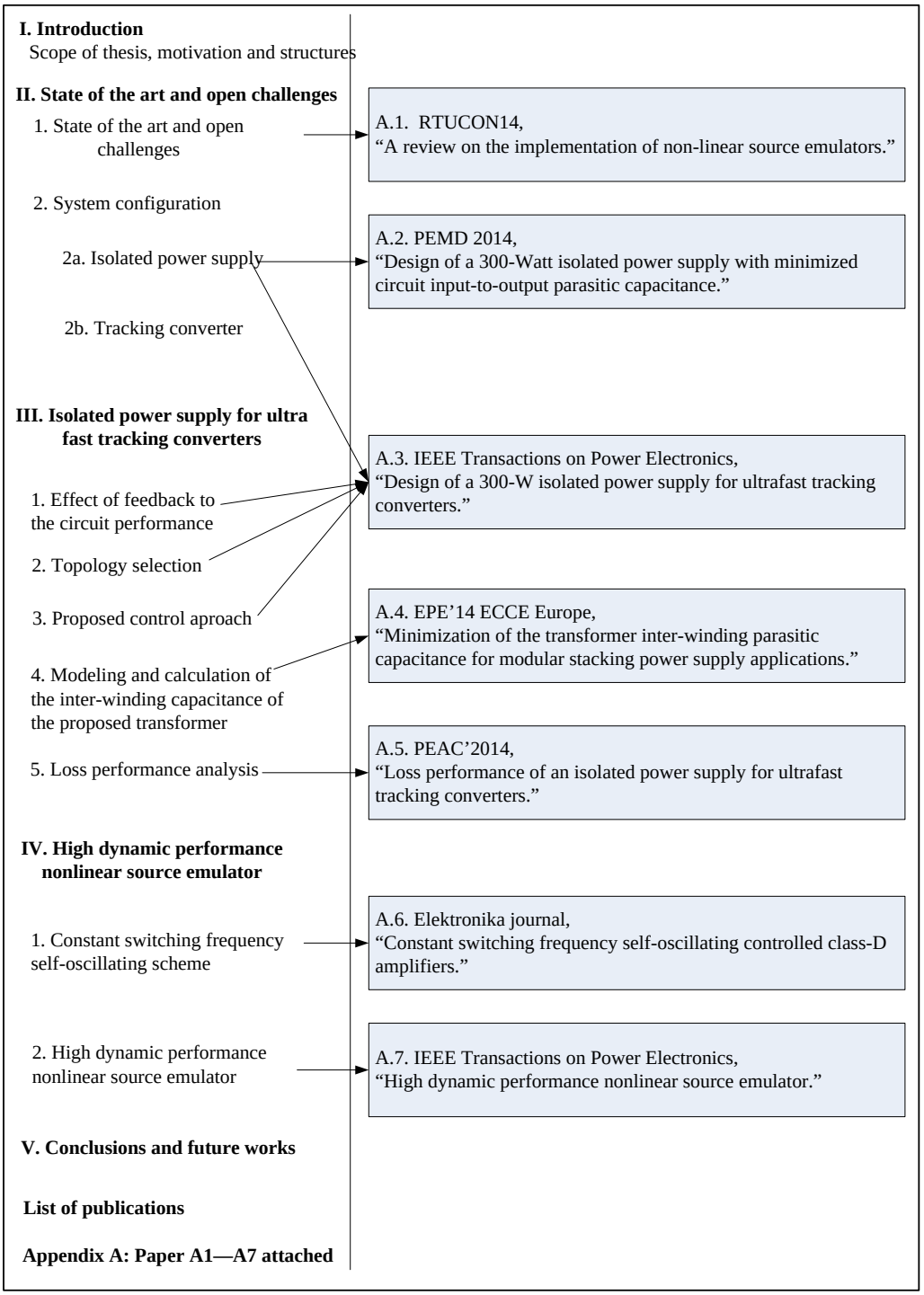


Figure 1.1: The complete thesis outline.

Chapter 2

State of the art and open challenges

2.1 State of the art and open challenges

In the test and development of renewable energy based converters, the use of non-linear source emulators (NSE) offers several advantages over the use of real non-linear sources. First, it requires a reduced test volume compared to the large non-linear source. Second, the cost of the test system with the NSE is usually less than the system with non-linear sources [7]. One of the examples is that, if non-rechargeable batteries were used in the testing, it would have to be disposed of after each test; hence, the testing is expensive, but a battery emulator based on a power electronics system could be reused for a long time. Finally, an NSE provides flexible and reproducible test conditions for the downstream converters because test conditions can be programmed or set inside the NSE [8; 9]. As a result, research on the development of NSE systems has been advanced recently.

Examples of the non-linear source are the fuel cell, battery, thermoelectric generator [10; 11], and electric energy from the sun or PV systems.

Considering a fuel cell system as a non-linear source, the static V-I curve of a fuel cell emulator can be represented by a third-order polynomial as [1; 2]:

$$V = f(I) = \alpha_3 I^3 + \alpha_2 I^2 + \alpha_1 I + \alpha_0, \tag{2.1}$$

where V is the fuel cell terminal voltage, I is the fuel cell output current, and α_0 to α_3 are the coefficients of the static V-I curve and they change according to the changes of hydrogen concentration. Fig. 2.1

Batteries are also used extensively in industry such as in electric vehicle (EV) or hybrid electric vehicle (HEV) applications [3; 12; 13]. A circuit model of a battery is shown in Fig. 2.2. The dashed box models a battery, in which, V_{oc} and R_i are the open-circuit voltage and internal resistance, respectively. The rest of the circuit models an output with an output filter capacitance C_l. The load is not necessarily fixed, it can vary over time with activities and power management policies [3; 13].

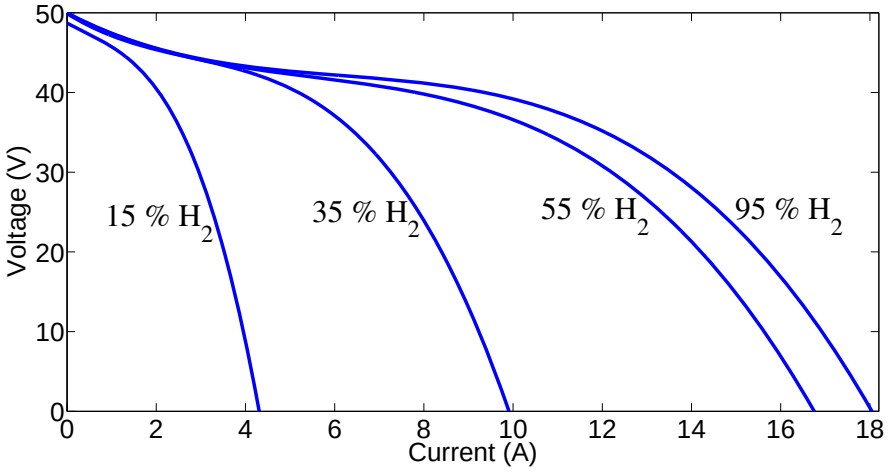


Figure 2.1: Changes of operating point due to changes of hydrogen concentration [1; 2]

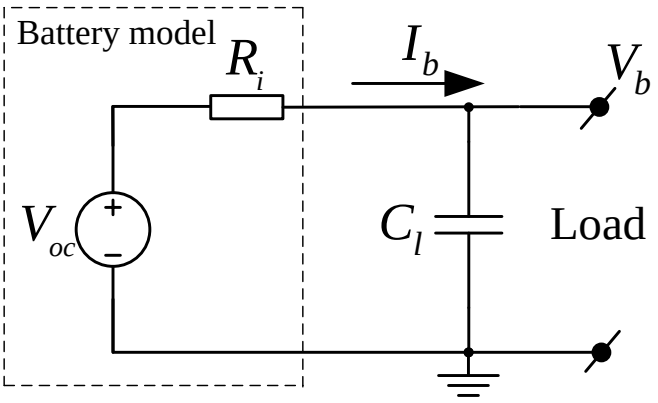


Figure 2.2: A circuit model of a battery [3].

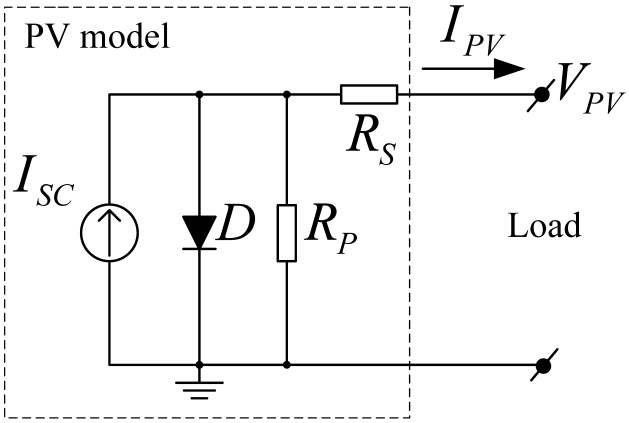


Figure 2.3: The five-parameter model.

The available voltage at the output of the battery is:

$$V_b = V_{oc} - IR_i. \tag{2.2}$$

During the discharge of the battery, V_{oc} decreases while R_i increases; both of them are dependent on the state of the battery and its internal temperature.

In case of a PV system, the *five-parameter model* [14; 15] is widely used to describe the system's electrical characteristics. The model is shown in Fig. 2.3. It is also called the *single diode model* [16; 17]. The current is related to the terminal voltage V_{PV} and the short circuit current I_{SC} by:

$$I_{PV} = I_{SC} - I_d(\mathrm{e}^{(\frac{V_{PV}+I_{PV}R_S}{nV_t})} - 1) - \frac{V_{PV} + I_{PV}R_S}{R_P}, \tag{2.3}$$

where R_P models the loss due to leakage currents across the junction, R_S models the internal series resistance, I_d is the dark saturation of the diode, V_t is the module thermal voltage, and n is the ideality factor, which falls in a range between 1 and 2. The short circuit current I_{SC} is affected by the sun irradiation. The open circuit voltage V_{OC} is affected by the cell temperature. Normally, R_P is relatively large and R_S is relatively small. In practice, the model can be reduced further to the *four-parameter model* [18] where the parallel resistor R_P is neglected. In some cases, the series resistor R_S is also neglected, resulting in a much simplified model, where:

$$I_{PV} = I_{SC} - I_d(\mathrm{e}^{\frac{V_{PV}}{nV_t}} - 1). \tag{2.4}$$

In paper A.7., the existing NSE control approaches can be classified into the following three categories.

The first category is the voltage-controlled approach. It is illustrated in Fig. 2.4. This is where the power circuit is a voltage-controlled amplifier. The output current is sensed and fed to a reference generator. The reference generator produces a reference output-voltage signal for the power circuit to amplify [1–3; 7–9; 12; 13; 19–31].

The second category is the current-controlled approach, where the power circuit is a current-controlled amplifier. The output voltage is sensed and fed to a reference

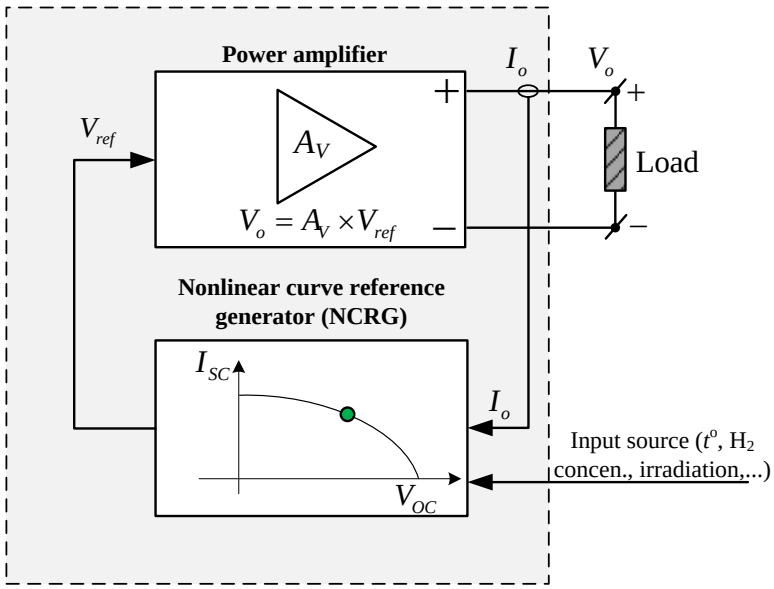


Figure 2.4: Block diagram of a voltage controlled NSE.

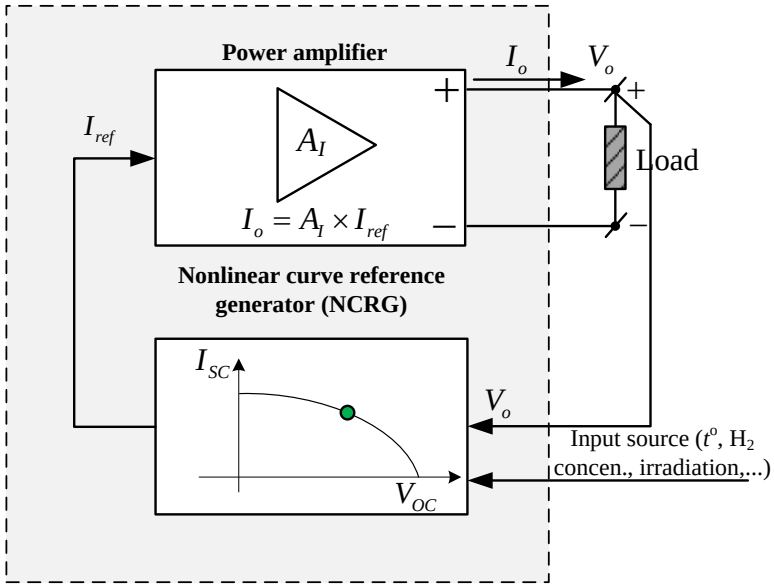


Figure 2.5: Block diagram of a current controlled NSE.

generator. The reference generator produces a reference output-current signal for the power circuit to amplify [32; 33]. This is illustrated in Fig. 2.5. In both categories, there is an *optional* input that represents the operating condition of the NSE. The condition can be temperature, hydrogen concentration, sunlight intensity, internal resistance, etc.

The third category is when both a current controlled and a voltage controlled power circuit are used [34]. In [34], a model-based NSE was developed. The authors used two separate power sources: a controllable linear voltage regulator and a controllable linear current regulator. The voltage regulator is active when the operating points are along the MPP to the open circuit point of the current-voltage

Table 2.1: Specifications and characteristics of existing fuel cell emulators

References	Power- (W) rating (W)	Power stage	Simulated-fuel cell	Dynamic load-change simulation	H_2 concentration-change simulation
[1; 2]	2 kW	Commercial PS	PEMFC	Yes	Yes
[19]	5 kW	Commercial PS	SOFC	Yes	Yes
[21]	Not found	Custom made	DMFC	Yes	No
[20]	500 W	Custom made	PEMFC	Yes	No

Table 2.2: Specifications and characteristics of existing battery emulators

Reference(s)	Power rating	Power stage	Simulated battery	Thermal model
[3; 13],	Not found	Adjustable linear regulator	Li-Ion	No
[12]	Not found	Bidirectional dc-dc converter	Li-Ion	No
[22]	Not found	Commercial power supply	Li-Ion	Yes
[23; 24; 35]	60 kW	Three phase interleaved buck	Not found	No

Table 2.3: Specifications and characteristics of existing PV emulators

Reference(s)	Step change of load settling time	Step load nom. to open	Step load nom. to short	Step change of input source	Power circuit
Koran 2010 [32]	3.8 ms (Fig. 17 of [32])	No	No	No	buck with LCLC filter
Kim 2013 [34]	100 ms (Fig. 15 of [34])	No	No	No	linear voltage & current regulators
Chang 2013 [29]	6 ms (Fig. 12 of [29])	No	No	No	LCLC resonant dc-dc converter
Koran 2014 [33]	3.2 ms (Fig. 15 of [33])	No	No	No	ac-dc three phase rectifier
Gadelovits 2014 [31]	8 ms (Fig. 15 of [31])	No	No	No	commercial power supply
Chang 2014 [30]	6 ms (Fig. 14 of [30])	No	No	No	LCLC resonant dc-dc converter
[7–9; 25–28]	Not found	No	No	No	linear power stage

(I-V) curve. In a complementary fashion, the current regulator is active when the operating points are along the MPP to the short circuit point. For hot-swapping operation (i.e, continuous transition from using one active power source to the other) when the operating points are close to the MPP, the two power sources are connected with two parallel diodes in order to block the reverse current that may flow from one power source to the other.

Table 2.1 summarizes the specifications and characteristics of the reviewed fuel cell emulators.

Similarly, Table 2.2 summarizes the specifications and characteristic of the existing

battery emulators in the literature.

The change of hydrogen concentration in a fuel cell system is analogous to the change of sunlight irradiation in a PV panel because they both cause a change in the short circuit current. However, there is a considerable delay from the change of the hydrogen concentration until the fuel cell reacts, whereas the change of sunlight intensity has an almost instantaneous effect to the operating point of a PV panel. Therefore, simulation of a fuel cell system requires less control bandwidth than simulation of a PV system. The partial shading effect of a PV system also complicates the simulation of a PV system. In general, most laboratory testing prototypes reported tend to try to resemble the most basic electrical characteristics of the non-linear source. They also tend to simplify or ignore the other characteristics such as the hydrogen concentration change in fuel cell emulators, the thermal behavior in battery emulators, and the partial shading effect in PV emulators.

Table 2.3 summarizes the characteristics of the existing PV emulators in terms of their dynamic performance.

It is noted that some ideal nonlinear sources will react instantly to a load step. The transient time is theoretically zero. In practice, a real PV panel can physically contain a source capacitance due to the diffusion capacitance of each PV cell [6]. This capacitance is in parallel with the diode and the parallel resistor. The value of this capacitor varies with the operating points of the PV panel. Typical value range of the source capacitance for a 312-W, 400×8 cm×cm silicon PV panel is from about 4 nF at the point close to the short circuit, to 6.7 μF at the open circuit [6]. The experimental source capacitance report in reference [6] is reproduced in Table 2.4. The data are plotted in Figs. 2.6 and 2.7.

The presence of a source capacitor makes the output current and voltage of a real PV panel under a load step take from hundreds of nanosecond to tens of microsecond in order to settle down [36]. This can also be verified by the following proposed estimation. Supposing the converter is experiencing a load step; the operating point is moving from the short circuit to a resistive load that corresponds to the operating point of (V_o, I_o)= (160 V, 0.982 A). Thus, $R = V_o/I_o = 163\ \Omega$. From Table 2.4, the source capacitance is $C = 107$ nF. Considering a current source of $I_{SC} = 1.07$ A constantly supplies a load which consists of a source capacitance C in parallel with a resistive load R, the output voltage as a function of time is:

$$v_o(t) = I_{SC}R(1 - \mathrm{e}^{\frac{-t}{RC}}). \tag{2.5}$$

The transient time for this PV system to move from short circuit $(0, I_{SC})$ to (V_o, I_o) is approximated by:

$$\Delta t = -RCln(1 - \frac{V_o}{I_{SC}R}) = 4.37 \times 10^{-5}\ s = 43.7\ \mu s. \tag{2.6}$$

By the same approximation method, it will take approximately 1.1 μs for this PV system to complete the transition from the short circuit to the operating point (V_2, I_2)= (60 V, 1.062 A).

However, as can be seen from Table 2.3, the best reported dynamic performance was 3.2 ms [33], which is a factor of hundred times slower than the actual dynamic response of a PV panel under dynamic tests.

Table 2.4: Dynamic variation of capacitance at different operating points [6]

PV array voltage	1.07 A short circuit current	2.339 A short circuit current	Capacitance @ 1.07 A short circuit current	Capacitance @ 2.339 A short circuit current
0 V	1.07 A	2.339 A		
40 V	1.066 A	2.332 A	4.062 nF	3.95 nF
60 V	1.062 A	2.326 A	4.046 nF	4.67 nF
80 V	1.057 A	2.317 A	4.342 nF	5.96 nF
100 V	1.049 A	2.303 A	5.051 nF	10.2 nF
120 V	1.036 A	2.281 A	6.705 nF	54.2 nF
140 V	1.017 A	2.231 A	13.74 nF	240 nF
160 V	0.982 A	2.125 A	107.3 nF	954 nF
180 V	0.898 A	1.771 A	609.5 nF	3.22 uF
200 V	0.634 A	0.964 A	2.694 uF	6.77 uF
216 V	0.133 A	0.0 A		

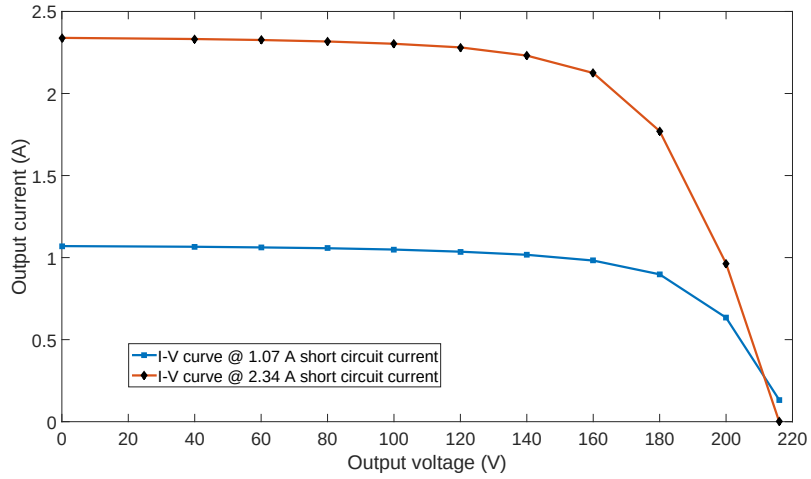


Figure 2.6: I-V curve generated from Table 2.4.

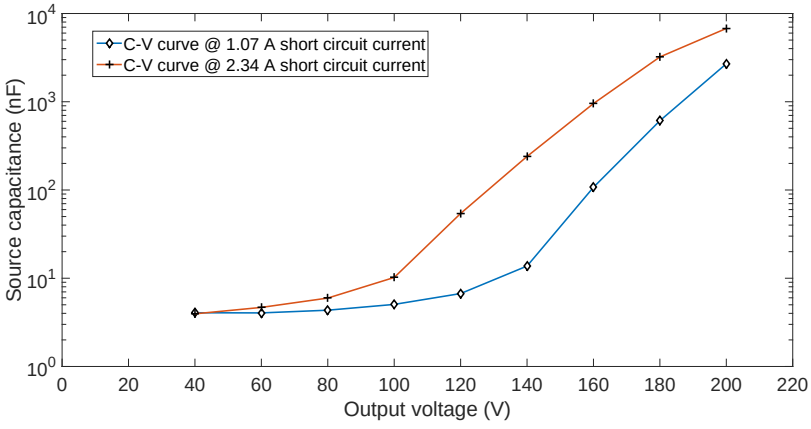


Figure 2.7: C-V curve generated from Table 2.4.

It is the aim of this project to develop a high dynamic performance NSE. The specifications of the proposed system will be presented in the next section.

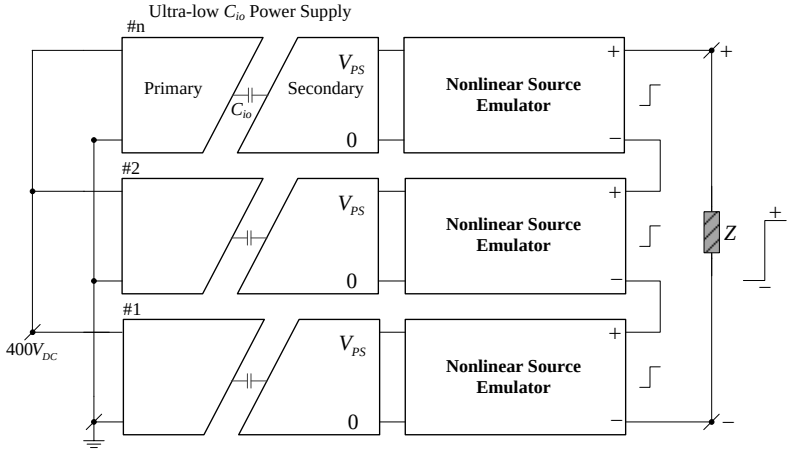


Figure 2.8: Block diagram of the proposed approach.

2.2 System configuration

The proposed system block diagram is shown in Fig. 2.8. A module of the proposed system consists of a power supply and a proposed high dynamic NSE. If higher power is desired, then multiple modules can be stacked together. With this modular approach, the proposed system can simulate different types of nonlinear sources with different power ratings ranging from the power of one module to multiple times of the power of one module.

The proposed NSE is designed to achieve a transient response within 10 μs.

2.2.1 Isolated power supply

Due to the fast output voltage regulation of the NSE, there will be a large amount of conductive common mode currents drawn from their output. These currents are linearly proportional to the input-output capacitance of the power supply.

$$i_{com} = C_{io}\frac{dv_{out}}{dt}. \tag{2.7}$$

These currents are drawn from the NSEs output. Therefore, they distort the output current waveforms of the NSEs, and the performance of the output is impaired. The adverse effects become worse when the number of stacked modules increases. Therefore, in order to achieve fast transient response at the output, the circuit input to output parasitic capacitance must be minimized.

A thorough discussion of the analysis, design, and development of the proposed isolated power supply is the main subject of chapter 3.

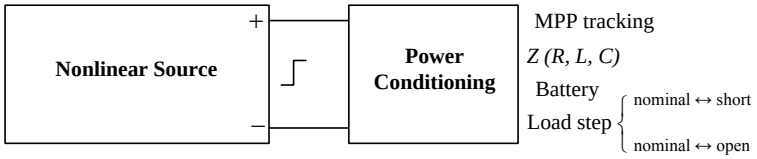


Figure 2.9: Connection between a nonlinear source emulator and a power conditioning unit.

2.2.2 Nonlinear source emulator

A load that connects with an NSE can take many different forms (see Fig. 2.9). A load can be a maximum power point tracker (MPPT) that tracks the maximum power point of the NSE. It can be an impedance such as an ohmic load, an inductive load or a capacitive load. It can be a battery to store energy from the NSE. It can also be a load step system that regulates output power such as a load step between nominal load and short circuit, or a load step between nominal load and open circuit. In load step regulation, the system is pulse width modulated and switching with high frequency (20 kHz or more). Since the bandwidth of the regulation is usually less than the switching frequency, pushing the switching frequency up has an advantage of allowing a higher control bandwidth. The switching frequency is constrained by the step response of the output of the NSE. Therefore, a step response is desired to be fast or in other word, the transient response should take as little time as possible. A sate-of-the-art transient response of 10 μs is the design goal of the NSE in this thesis.

In short, there are two requirements that make a state-of-the-art NSE:

- High dynamic performance (tens-of-microsecond transient responses).
- Low output (voltage and current) ripple.

The first, also the most important requirement, is the dynamic response. The goal of this project is to make an NSE that has a transient response of 10 μs. The second requirement is the very small output voltage ripple. A practical nonlinear source does not produce any output voltage or current ripple at its output. If the power circuit of the NSE is a switch-mode power converter, it is very difficult to attain zero output ripple, unless either an infinite switching frequency is used or the output filter corner frequency is zero. In fact, these two conditions are not feasible. Therefore, a more reasonable ripple is aimed by this project. The peak-to-peak output voltage ripple is targeted at 0.1 % of the maximum output voltage. If a non-isolated buck converter is used as the main power circuit, then the dc rail voltage is the maximum output voltage.

Table 2.5 summarizes the specification of the proposed NSE. Chapter 4 will discuss the proposed NSE in detail.

Table 2.5: Specifications of the proposed nonlinear source emulator

Transient response	10 μs
Maximum output voltage ripple	0.1 %V_{max} (60 mV for V_{max}=60 V)

Chapter 3

Isolated power supply for ultrafast tracking converters

In this chapter, the very low circuit input-to-output capacitance (very low C_{io} isolated power supply will be discussed. The detail of the discussions, findings and results can be referred to paper A.2, A.3. The modelling of the iterwinding capacitance of the proposed current transformer can be found in paper A.4. The loss performance of the power supply can be found in paper A.5.

3.1 Introduction

In an isolated power supply, the element that predominantly contributes to the circuit total input-to-output parasitic capacitance is the transformer [37–41]. Therefore, many studies have focused on mitigating CM noise by minimizing the inter-winding capacitance of the transformer [37; 41–44]. The existing transformers in existing power converters up to 1.2 kW have their inter-winding capacitance in the range of several tens of picofarads for low output power converters to hundreds of nanofarads for higher power ratings. For example, the existing transformer in a 1.2 kW converter is reported to have 1.5 nF inter-winding capacitance [45]. An E-core transformer used in a flyback converter with a power rating of 30 W is reported to have 34 pF of inter-winding capacitance [46]. The inter-winding capacitance per unit output power is approximately 1 pF/ W.

In this chapter, we propose a topology that can achieve an inter-winding capacitance per unit output power of 0.033 pF/ W, which is 30 times smaller than existing works [45; 46]. Table 3.1 shows the specifications of the proposed 300-W prototype.

Table 3.1: Design specification

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Circuit input-to-output capacitance	10 pF

3.2 Effect of isolated feedback to the circuit performance

In controller design of isolated converters, the feedback elements must provide electrical isolation to the control feedback paths and be able to transfer information as quickly and accurately as possible. Examples of such elements are optocouplers and signal-level isolation transformers. However, these components possess several undesirable attributes that need to be taken into account.

For the optocoupler, there are two main disadvantages. First, they have very low bandwidth and limited accuracy that lower the converter's overall bandwidth and might inhibit fault protection of the circuit. The typical value of the bandwidth of a commercially available optocoupler used in power supplies is less than 5 kHz [47]. Second, the input-output coupling capacitance inherent in an optocoupler will add to the overall circuit input-to-output parasitic capacitance. Its capacitance is typically in the range of nanofarads [47]. Therefore, an optocoupler is not a suitable candidate for the targeted applications.

Signal-level isolation transformers have better bandwidth than the optocoupler, but they have higher coupling capacitance. The typical coupling capacitance of a signal-level transformer is from 2 pF [48] to 12 pF [49], which will add 20 % and 120 % to the total circuit input-to-output capacitance, respectively. Hence, the use of an isolation transformer in feedback is not acceptable in such applications.

In summary, the control approach which uses feedback paths across the isolation boundary is not optimal where minimization of circuit input-to-output parasitic capacitance is the primary goal.

3.3 Topology selection

Based on the awareness of the effect of isolated-feedback on the circuit performance, a power supply suitable for ultrafast tracking converters must possess the following features:

- Low circuit input-output capacitance.
- Reduced number of crossings of the isolation barrier.

The first requirement implies a loosely coupled transformer to be used. However, in magnetic components, the leakage inductance and the inter-winding parasitic

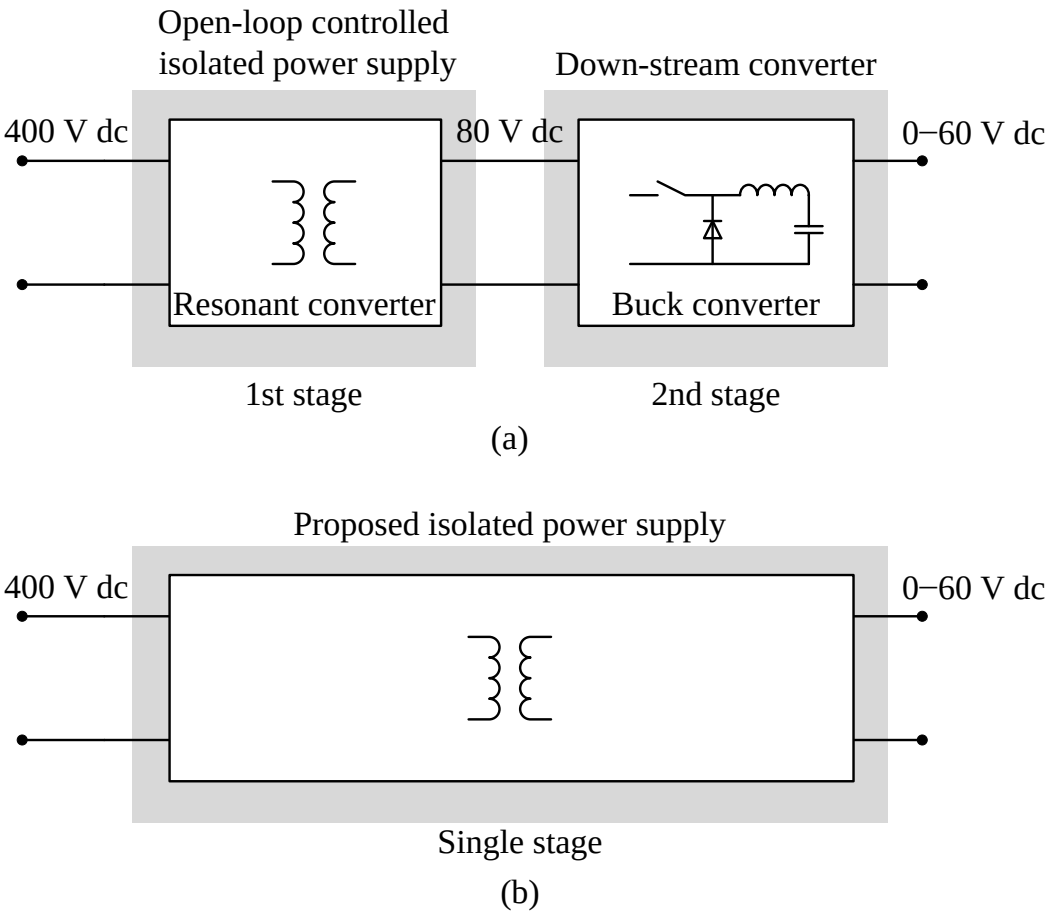


Figure 3.1: Minimized circuit input-output capacitance systems: a) two-stage solution with existing topologies, b) one-stage solution with the proposed topology.

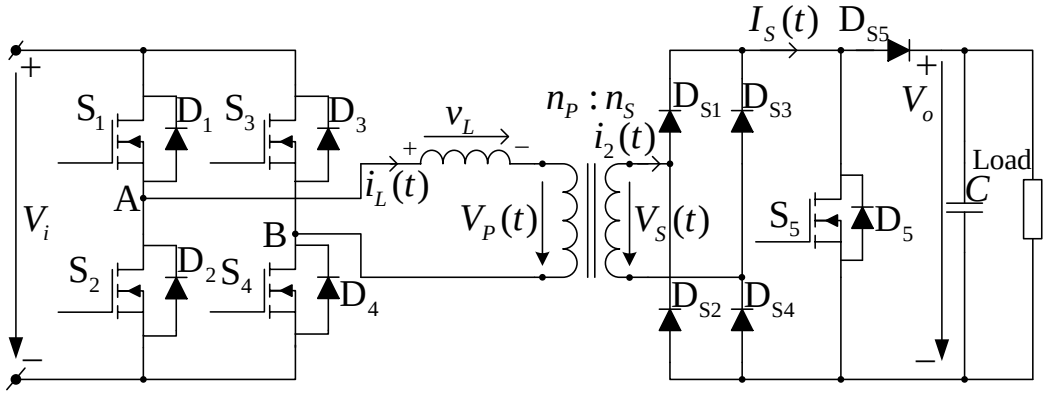


Figure 3.2: Topology of the proposed converter.

capacitance are inversely proportional to each other [50]. Conventional full-bridge converters such as buck- or boost-derived converters are not suitable for these applications. This is because, in those topologies, the transformer requires low leakage inductance and consequently high inter-winding capacitance due to the close proximity requirement between windings. This will increase the total circuit input-output capacitance. Furthermore, those topologies usually involve the use of feedback elements crossing the isolation boundary and thus violate the aforementioned second requirement.

The relatively high transformer leakage inductance due to the loose coupling can be useful in resonant topologies [51–53]. This suggests an approach shown in Fig. 3.1a, based on a two-stage converter. The configuration utilizes only standard existing topologies. The system is powered by a power factor correction whose output voltage is assumed to be 400 V dc. The resonant converter operates with open-loop control to eliminate the feedback from output to the input. Its output voltage is used to supply a non-isolated down-stream converter, such as a buck converter, as demonstrated in Fig. 3.1a. The closed-loop regulation of the final output voltage is performed by the down-stream converter, while the low circuit input-to-output capacitance is determined by the loose coupling and feedback-free operation of the resonant converter. For example, if the down-stream buck converter has a maximum output voltage level of 60 V, then the resonant converter can be designed for a voltage output of about 80 V. In short, in order to attain the two aforementioned goals, it must be done with a two-stage converter with a separate control loop for each stage. This approach, however, can be costly and require significant effort to develop a separate control loop for each stage.

Considering the control performance, a feedback-free resonant converter design is only optimal if the switching frequency is fixed at the load-independent frequency, where the converter gain is independent of variation in the load. However, this creates disadvantages if the open-loop control fails to track the load-independent point due to the tolerances of the control and sensing circuits as well as of the power circuit. The variation of the voltage gain around the vicinity of the load-independent point can cause the voltage to fail. Moreover, the regulation of the down-stream converter speed is limited by the output filter used.

This thesis proposes a converter and control that combine two stages into one stage. The concept is shown in Fig. 3.1b. The proposed converter and its control is free from feedback across the isolation boundary. However, the output voltage is locally controlled by a closed loop in the secondary side, and thus it maintains the high performance and robustness against the control circuit tolerance and circuit parameter variation. The proposed converter topology is shown in Fig. 3.2

The transformer structure, modelling and validation will be presented in Section 3.4. The detailed analysis of the control approach will be presented in Section 3.5.

3.4 Transformer structure, interwinding capacitance modelling and validation

In this section, the transformer structure, its specification and its inter-winding capacitance mathematical model will be presented first. After that, key measurement data including the transformer's primary to secondary winding impedance, the interpreted transformer's inter-winding capacitance, and the leakage inductance referred to the primary side will be given.

3.4.1 Transformer structure

The general structure of the proposed transformer is illustrated in Fig. 3.3a and the transformer prototype photo is shown in Fig. 3.3b. The winding with fewer turns will be placed in the geometrical center of the core, forming a rectangular frame. The remaining winding with more turns is tightly wound around the core. This is respectively the case of the secondary winding and primary winding in Fig. 3.3. With this structure, the two windings are separated from each other by a reasonably large distance. Moreover, the die-electric material between them is only the surrounding air that has the second lowest permittivity to vacuum. All of these features result in the transformer's extremely low inter-winding parasitic capacitance.

The specifications of the developed transformer are provided in Table 3.2. It also provides dimensional information about the core and winding with respect to the notations in Fig. 3.4. It is a R36/23/15 toroid core from Epcos with N87 material. The primary winding is made by Litwize with 60 0.2 mm-diameter twisted parallel wires. The secondary winding uses copper wire with a 1 mm diameter. The turns ratio is 55:11.

3.4.2 Mathematical model of the inter-winding capacitance

The inter-winding capacitance can be calculated by using the stored electric energy method [54–59], in which voltage distribution plays a vital role. The detail can be found in section V of paper A.4. or in paper A.5. The argument of this method is that the total stored electric energy between two windings are equal to the electric energy stored in each different part of the windings. Hence:

$$E_{total} = E_i + E_o + E_B + E_{Cin} + E_{Cout} = \frac{1}{2} C_{int} (V_P - V_S)^2. \tag{3.1}$$

The energy stored by each part can be calculated (see paper A.4. [59] or A.3. [60]), so the total stored energy E_{total} can be derived. In addition, the voltages across the winding terminals, V_P and V_S, are known. Therefore, we can calculate the interwinding capacitance C_{int} as:

$$C_{int} = \frac{2E_{total}}{(V_P - V_S)^2}. \tag{3.2}$$

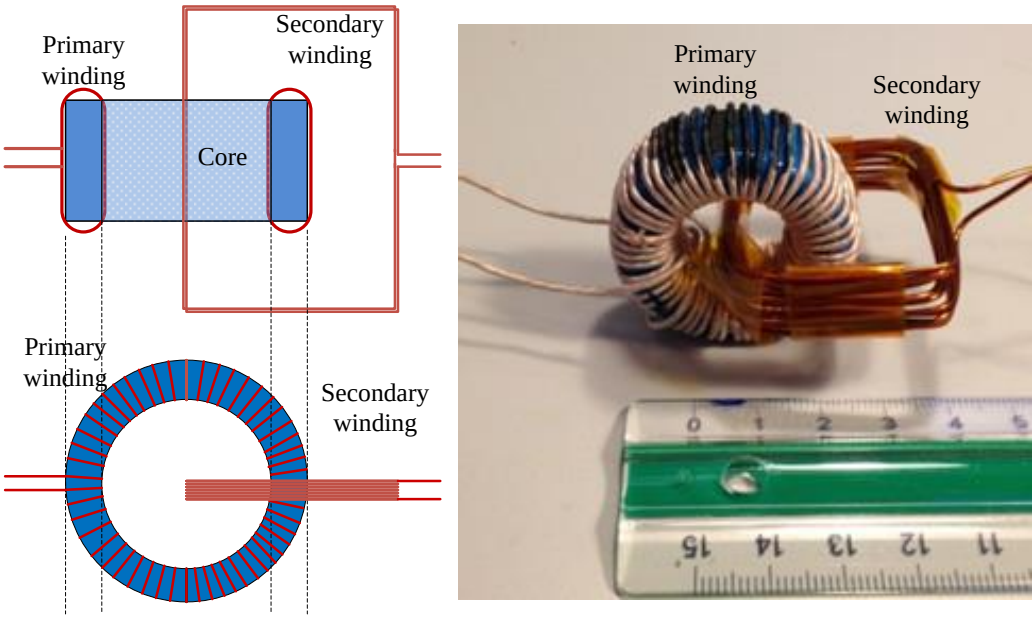


Figure 3.3: Transformer structure. (a) conceptual structure top and side view; and (b) the transformer prototype.

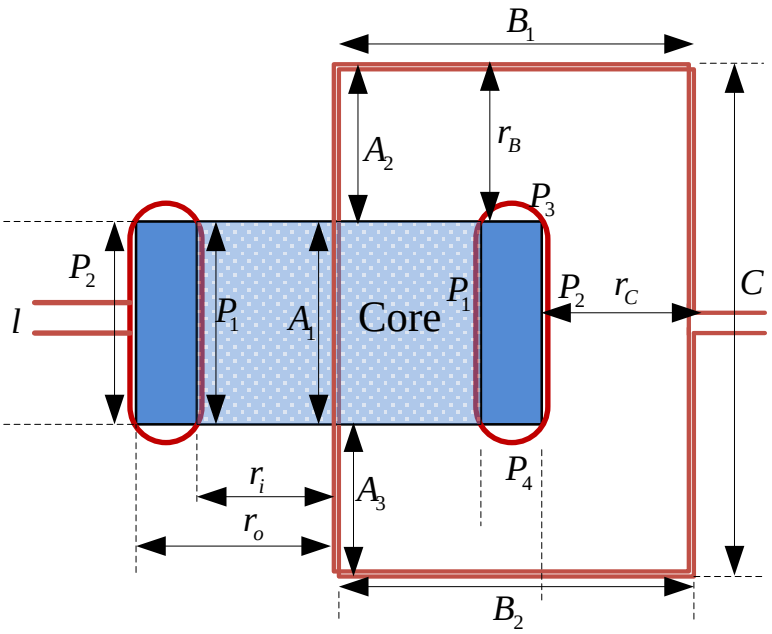


Figure 3.4: Proposed transformer structure and geometry.

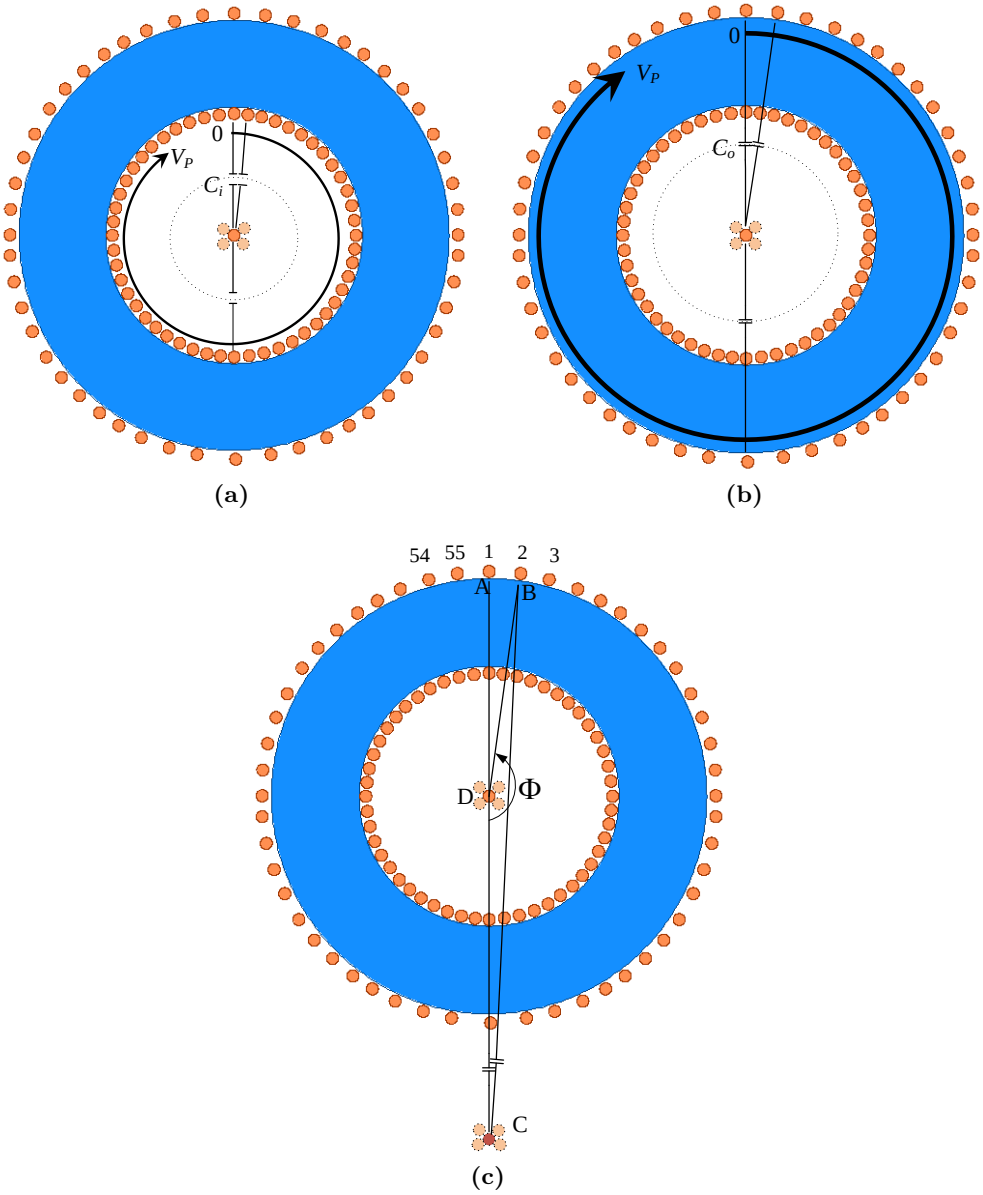
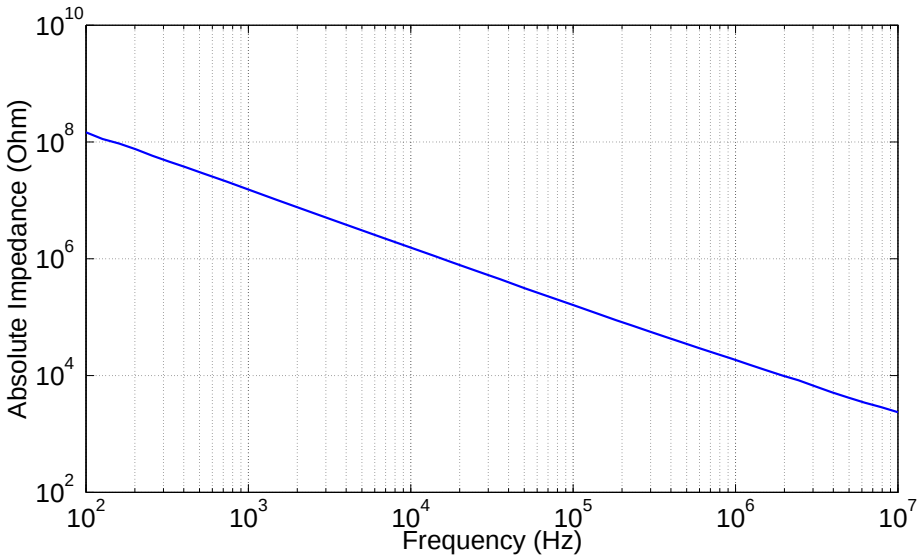
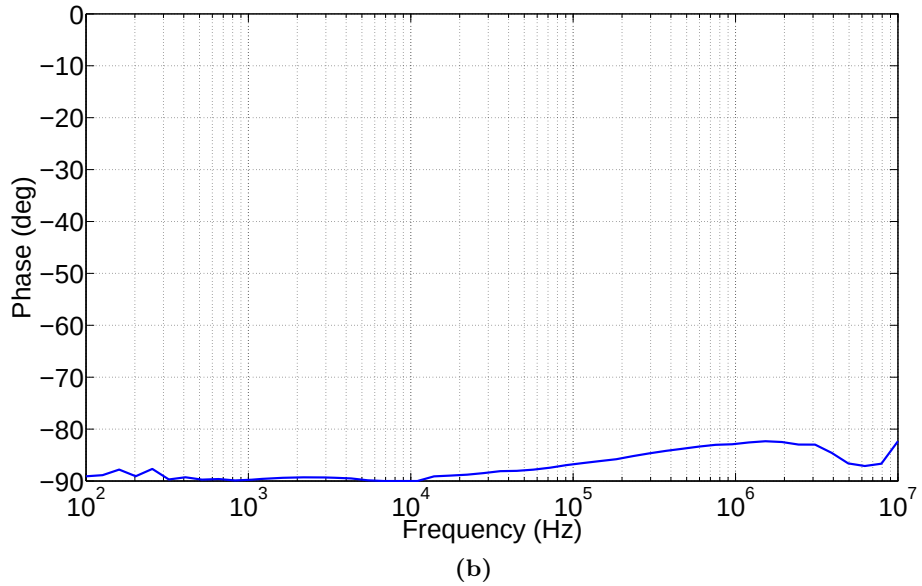


Figure 3.5: Effect of parasitic capacitance from the secondary winding of (a) segment A to the inner ring of the primary winding; (b) segment A to the outer ring of the primary winding ; (c) segment C to the outer ring of the primary winding.

The calculated inter-winding capacitance, C_{int}, based on the parameters in Table 3.2 is 10 pF. It is observed from the calculated results in paper A.4. and A.5., that segment A_1 dominates the stored energy, and the contributions of segments B_1 and B_2 are negligible. The design guideline is that increasing the core geometry and increasing distance from segment C to the core will effectively reduce the inter-winding capacitance.



(a)



(b)

Figure 3.6: Inter-winding impedance measurement: (a) magnitude, (b) phase.

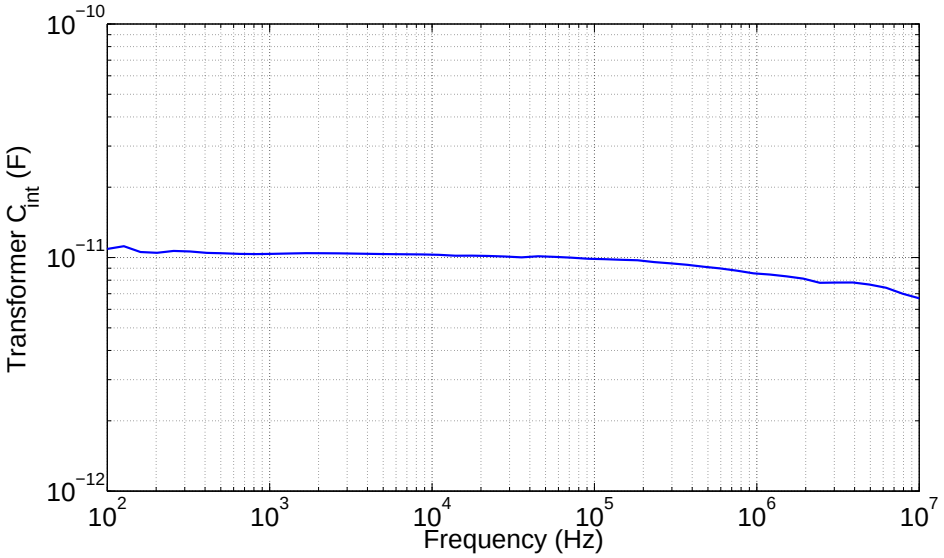


Figure 3.7: Measured inter-winding parasitic capacitance.

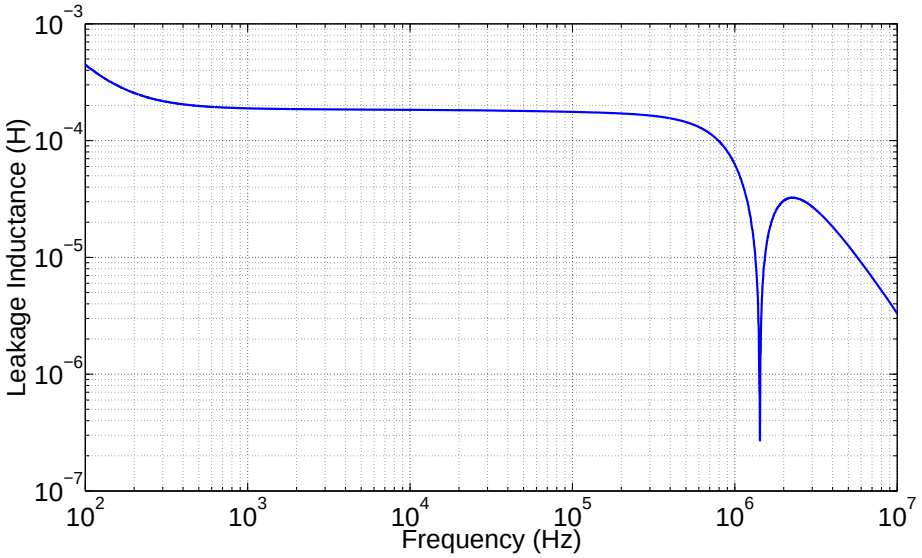


Figure 3.8: Measured primary side leakage inductance.

Table 3.2: Parameters of magnetic core and winding geometries of the transformer

Core material	N87
Core dimension	36 mm × 23 mm × 15 mm
Turns ratio	55:11
Primary winding	Litz-wire 60 × 0.2 mm
Secondary winding	copper 1.0 mm
ϵ_0	$8.85.10^{-12}$ F/m
d	1 mm
l	16 mm
r_i	11.5 mm
r_o	18 mm
n_p	55
n_s	11
V_P	300 V
V_S	60 V
r_B	12 mm
l_B	6.5 mm
l_C	16 mm

3.4.3 Measurement results

Fig. 3.6 shows the experimental data of the inter-winding impedance magnitude and phase of the transformer. The measured data are imported into MATLAB and processed by proper scripts to yield the interpreted coupling capacitance, whose values are shown in Fig. 3.7. It can be seen that the capacitance value is around 10 pF in the wide range of frequency from dc to 10 MHz. It is validated that with the proposed configuration of the transformer, an extremely low inter-winding parasitic capacitance can be achieved.

The process is repeated for the measurement of the impedance between two terminals of the primary side while the two terminals of the secondary side shorted. This impedance can be modelled as a leakage inductor. The impedance magnitude and phase can be found in Section 4 of paper A.2 or Section V of paper A.3. The measured magnitude of the leakage inductor is shown in Fig. 3.8. The leakage inductance value is 170 μH in the range of 100 kHz to 300 kHz. The consequential relatively high leakage inductance may be explained by the large geometrical separation of the two windings that produces relatively large leakage flux outside the core. Hence, the proposed topology as well as its associated control approach must be designed to utilize the leakage inductor. The control approach will be presented in the next section.

3.5 Proposed control approach

The detail discussions of the proposed control approach can be found in [60; 61], i.e., paper A.2. and A.3. in the appendix. They are summarized briefly here.

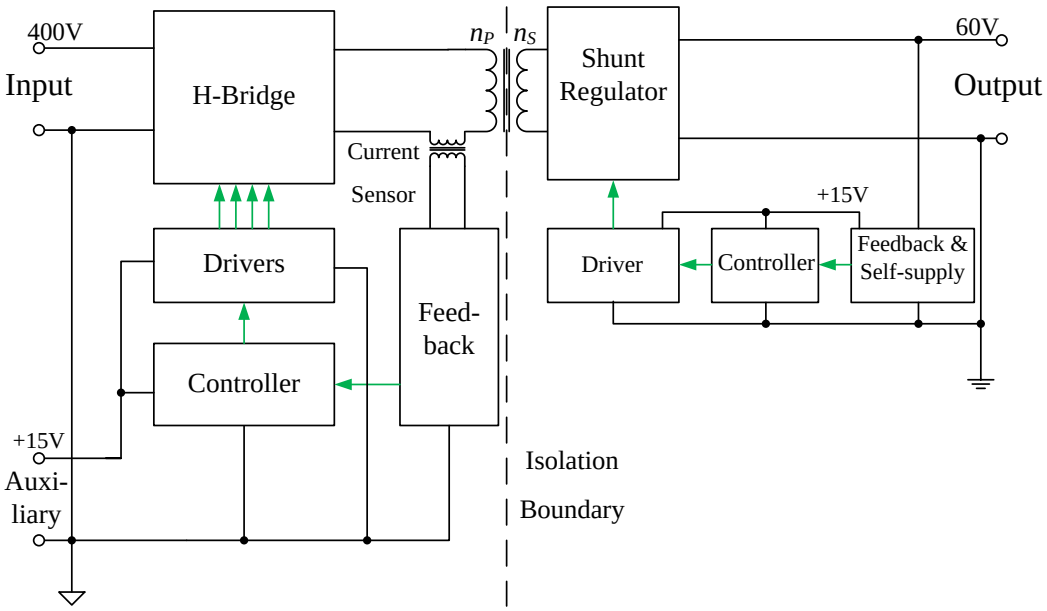


Figure 3.9: Block diagram of the circuit layout.

In this work, the control approach without isolated feedback is adopted in order to achieve minimum circuit input-to-output parasitic capacitance for the requirements of the targeted applications. The proposed converter physical configuration is shown in Fig. 3.9. There are two control loops where one resides in the primary and the other one resides in the secondary. The secondary side controller regulates the output voltage to be constant at 60 V. The primary side controller controls the primary-side inductor current; thus, it indirectly regulates the nominal output current. The secondary side circuit can be seen as a current source supplying the output capacitor in parallel with the load.

On the secondary side, the output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch the shunt switch S_5 on and off. When S_5 is switched off, the converter operates in its *power mode*; the output voltage increases. Vice versa, when S_5 is on, shunting the secondary side, the converter operates in its *shunt mode*; the output voltage decreases. This control approach is different from the control method of the conventional full-bridge topology or single active bridge topology in that the output voltage regulation is independent from the regulation of the active switches of the primary side.

On the primary side, because the leakage inductance is relatively high, at 170 μH, it is utilized as the main inductor in the circuit and there is no external inductor added. In this way, the leakage inductor, although being relatively high inductance value compared to a traditional converter, has become an integral part of the converter. The primary side inductor current can be controlled by adjusting one variable among the three variables of the primary switches: frequency, phase shift, and duty cycle. In this work, the frequency modulation is chosen. The duty cycle of the switches is fixed at 50 %, and the phase-shift is therefore at zero degrees. The primary side current i_L is first sensed and rectified. It is then low-pass filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analogue proportional-integral (PI) compensator. The output

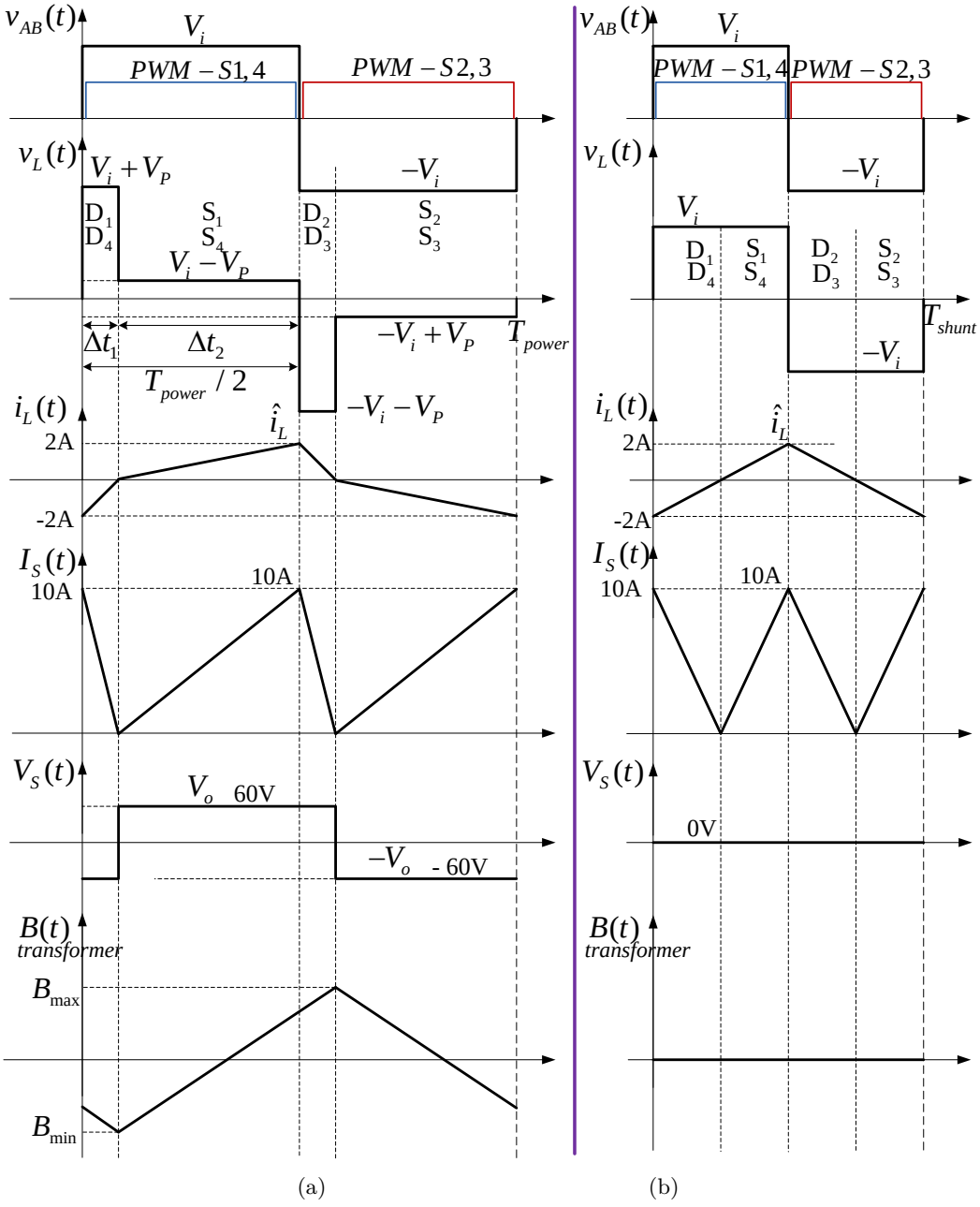


Figure 3.10: Analytical waveforms when the converter operates in: (a) power mode; and (b) shunt mode.

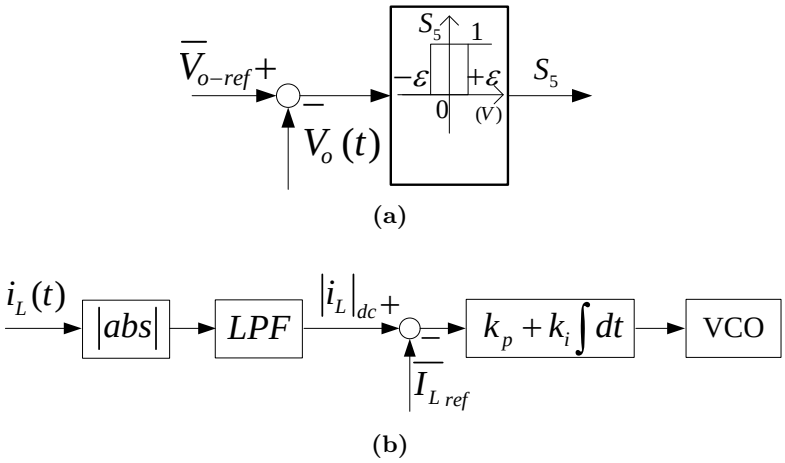


Figure 3.11: Control block diagram. (a) hysteresis control in the secondary side; and (b) average current mode control in the primary side.

of the PI compensator is fed to a voltage-controlled oscillator (VCO) that automatically adjusts the switching frequency to keep the rectified primary dc current to be a constant 1 A dc. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc. The analytical waveforms of the converter in the two operation modes are shown in Fig. 3.10; whereas, the block diagrams of the two control loops are shown in Fig. 3.11.

3.6 Loss performance analysis

Paper A.5. [62] discusses the loss performance of the proposed isolated power supply. We will not repeat the discussion here, but we are going to summarize the results and conclusions from paper A.5.

The calculated and measured results are shown in Figs. 3.12, 3.13, and 3.14.

The calculated results show that the primary side switching loss is the predominant loss in the converter. Therefore, in order to further improve the efficiency of the converter, it is suggested that future design focus on reducing the switching loss on the primary side. It may be achieved by selection of different MOSFET part that is faster and hence yields lower switching loss.

3.7 Experimental results

The most important experimental results are briefly summarized here. The less critical details such as measurement calibration (precision) and so on, can be found in the "Experimental Results" section of paper A.2. or A.3.

The circuit input-to-output capacitance is measured by the Agilent 4294A precision impedance analyzer. The two input terminals are shorted and so are the two output terminals. After that, the ground planes of the primary side and secondary side are measured with the instrument. Fig. 3.15 shows the circuit input-to-output

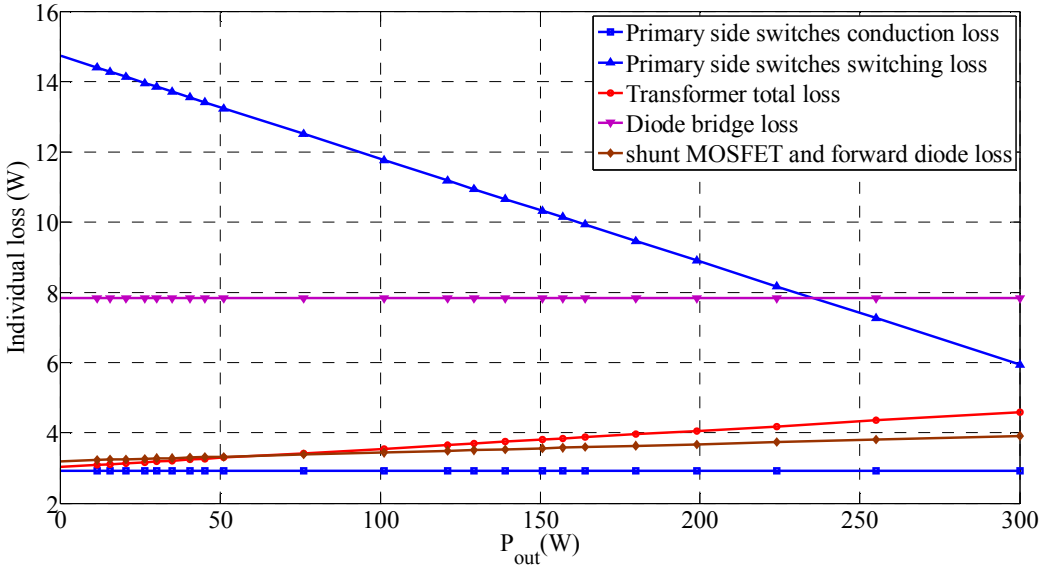


Figure 3.12: Converter's calculated breakdown loss.

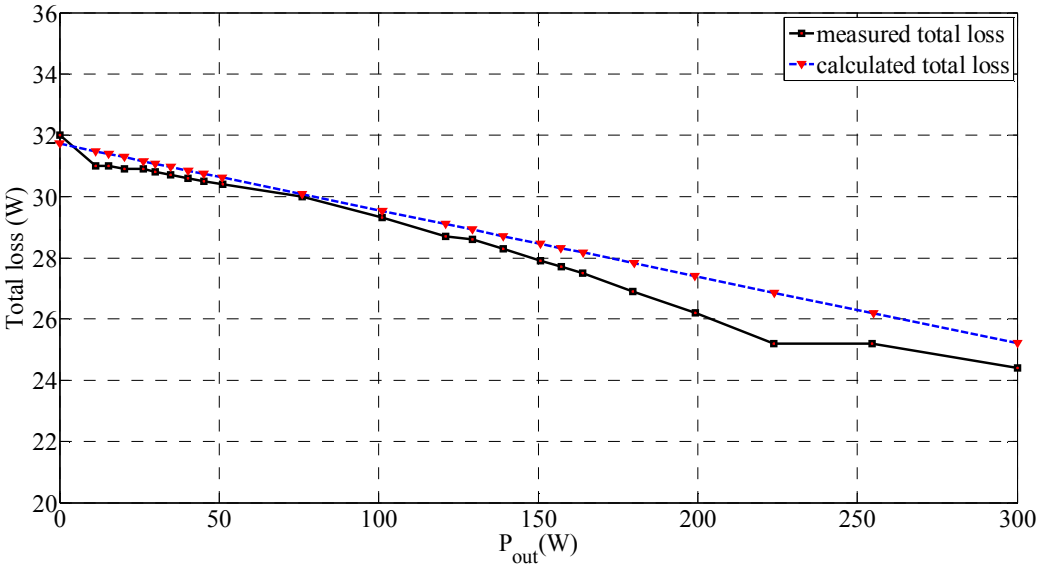


Figure 3.13: Converter's measured and calculated total loss.

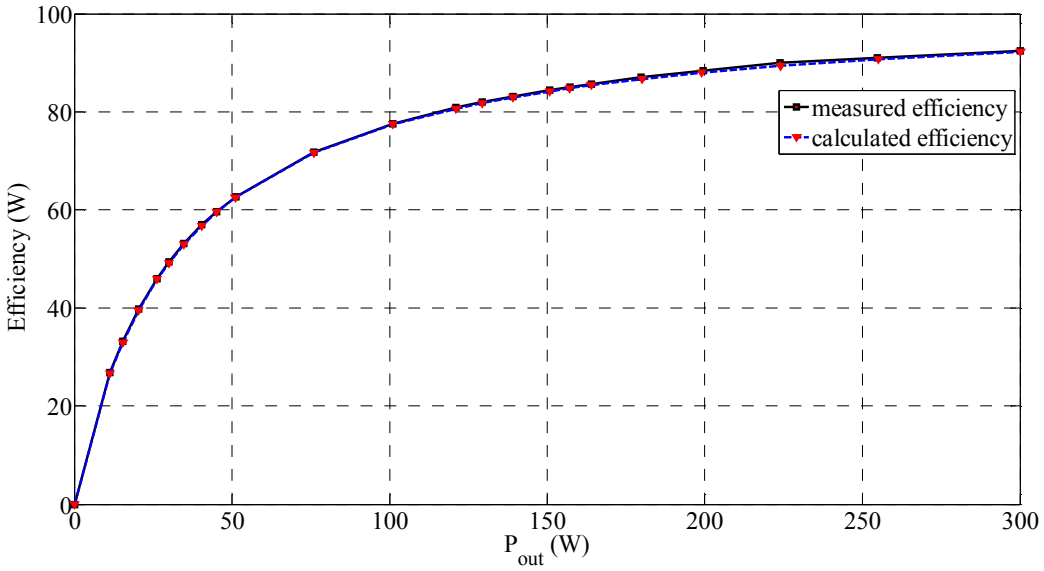


Figure 3.14: Converter's measured and calculated efficiency.

impedance magnitude and phase measurement. Its magnitude slope of -20 dB/dec and phase around $-90°$ makes it appropriate to model as a capacitor. The measured value of the capacitance is around 10 pF, which is shown in Fig. 3.16. In short, an extremely low value of circuit input-to-output capacitance has been achieved and it has been proven to be dominated by the inter-winding parasitic capacitance.

Fig. 3.17 shows the transient response from power mode to shunt mode. In a similar way, the transient from shunt mode to power mode is shown in Fig. 3.18. The value of the output voltage threshold, ε, is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady state values, which are 2 A peak and 60 V dc, respectively. The transient of the current from power mode to shunt mode and vice versa finishes within about 30 μs and 40 μs, respectively. The time needed for the inductor current to settle is mainly determined by the dynamic of the average current control scheme described in Fig. 3.11. The transient and steady state are both stable and satisfactory. The behaviour of the circuit matches accurately with the aforementioned circuit analysis.

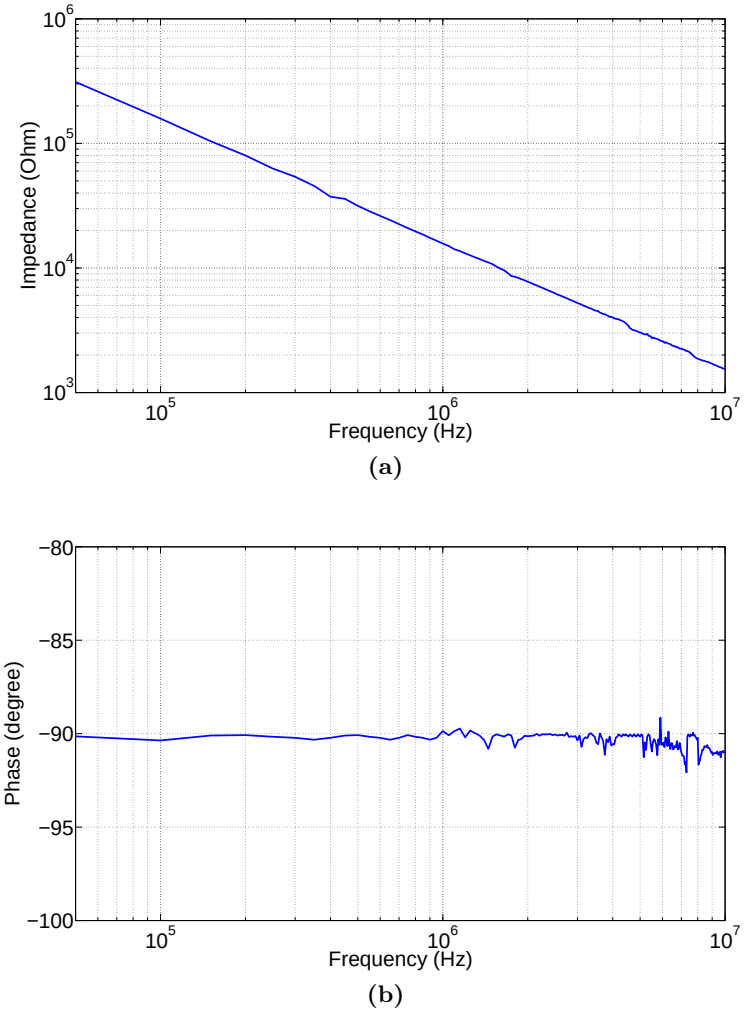


Figure 3.15: Circuit input-to-output impedance measurement: (a) magnitude; (b) phase.

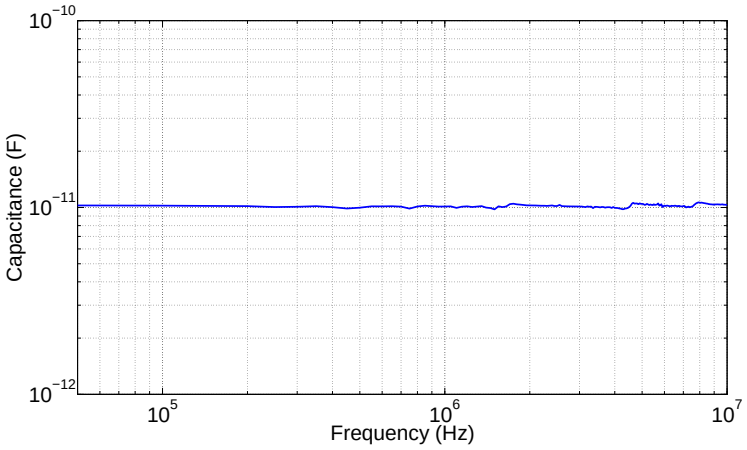


Figure 3.16: Circuit input-to-output parasitic capacitance.

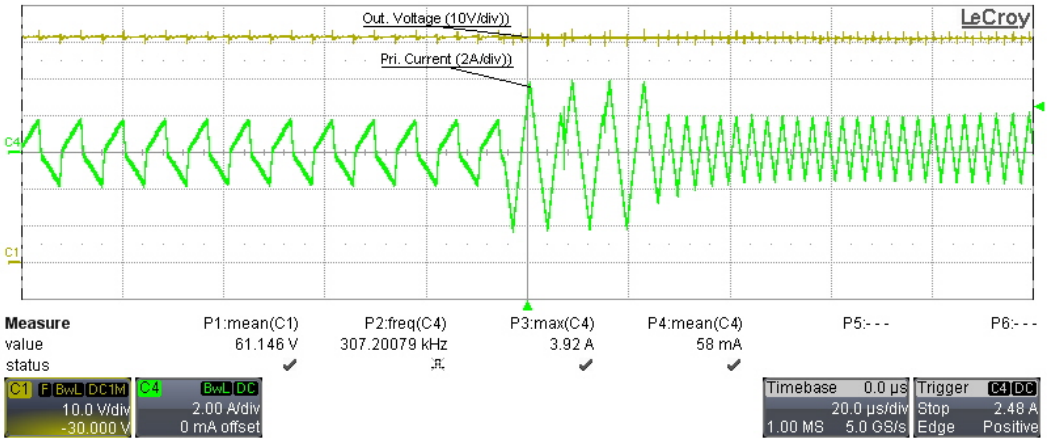


Figure 3.17: Transient response from power mode to shunt mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

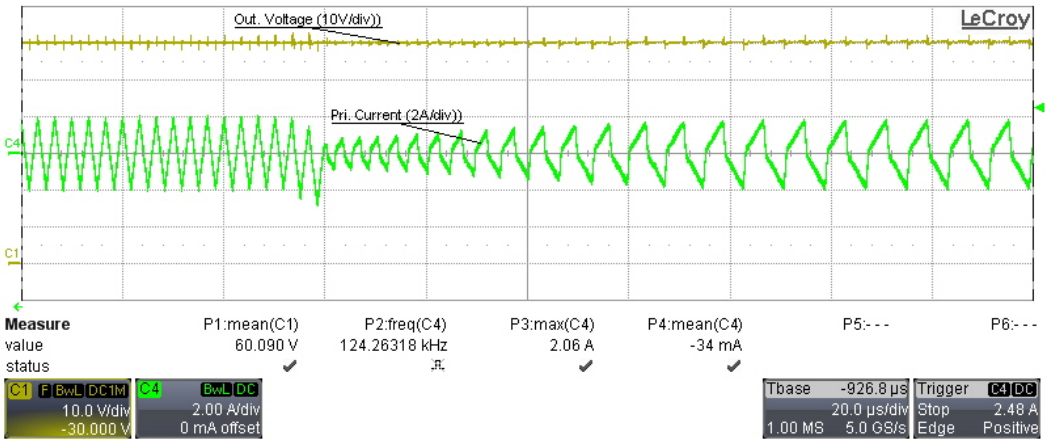


Figure 3.18: Transient response from shunt mode to power mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

Chapter 4

High dynamic performance nonlinear source emulator

4.1 Introduction

As stated in Chapter 2, Table 2.3, the goal of the proposed NSE is to achieve a transient response of 10 μs and a maximum output voltage ripple of 0.1% V_{max}, where V_{max} is the maximum output voltage that the NSE can produce. In order to achieve the desired transient response of 10 μs, the converter has to have a high control bandwidth. In order to achieve a low output voltage ripple and at the same time, not to compromise the efficiency, the proposed NSE will be developed based on a switch-mode converter. The output voltage ripple will be the residual of the pulse width modulated (PWM) power signal after filtered by an output filter stage.

Considering the transfer function of a second order LC output filter in a typical buck converter:

$$G_{filter-2nd}(s) = \frac{1}{LCs^2 + \frac{Ls}{R} + 1} = \frac{1}{(\frac{s}{\omega_0})^2 + \frac{s}{\omega_0 Q} + 1}, \tag{4.1}$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$ is the natural frequency, $Q{=}R\sqrt{\frac{C}{L}}$ is the quality factor, and R is the impedance of the load (assuming a resistive load).

Well above the natural frequency of the output filter, the filter magnitude is proportional to a square of the ratio of the natural frequency to the fundamental frequency, which is [63]:

$$|G_{filter-2nd}(j\omega)| \approx (\frac{\omega_0}{\omega})^2. \tag{4.2}$$

From equation 4.2, if for any reason, the switching frequency drops, then the magnitude out of the filter at the new switching frequency will increase rapidly. The output voltage ripple therefore increases. If the converter is to operate at different switching frequencies, then the lower switching frequencies will produce higher

output voltage ripples. It is therefore desired that the switching frequency be kept above a minimum value where the ripple requirement is still satisfied.

The dynamic performance of a switch-mode converter is significantly influenced by its modulation scheme. Modulation strategies can be classified into analogue modulation and digital modulation. The analogue modulation usually has better performance due to the absence of propagation delay or quantization error, which are inherent in digital modulation. There have been two basic analogue modulation methods in the literature, namely the triangular carrier-based modulation method and the self-oscillating modulation method. The self-oscillating modulation method possesses several advantages over the triangular carrier based method. One of the most important advantage is that it allows the open-loop control system magnitude to cross the 0 dB point precisely at the oscillation frequency, providing higher control bandwidth than a system with triangular carrier based modulation that needs to obey the Nyquist criterion.

For that reason, a self-oscillating modulation scheme is adopted in the development of the NSE in this project. However, one major drawback of a self-oscillating modulation scheme is that the switching frequency is dependent on the PWM duty cycle, i.e., the ratio of the time when the PWM signal is ON to a complete period. The switching frequency is approximately a parabolic curve with respect to the duty cycle. According to [63; 64], the switching frequency of a hysteresis self-oscillating modulated converter can be expressed by:

$$f_{sw} = \frac{K_{sw} D(1-D)}{\varepsilon}, \tag{4.3}$$

where ε is the height of the hysteresis threshold (also called hysteresis window), K_{sw} is a constant dependent on the circuit gain, and D is the duty cycle of the PWM signal. Fig. 4.1 shows the variation of switching frequency versus change in duty cycle of a hysteresis self-oscillating modulated converter. It can be seen that the switching frequency is maximum at the centre duty cycle of 0.5 and it drops rapidly with the change of duty cycle away from the centre duty cycle. For example, when the duty cycle is 0.1 or 0.9, the switching frequency drops 64 %, or nearly two thirds from the highest switching frequency. From equation 4.2, the attenuation at duty cycle of 0.1 drops 2.44 times, making the output voltage ripple increases about 2.44 times compared to that at the duty cycle of 0.5.

For all these reasons, in the development of a high bandwidth, low voltage ripple NSE, a self-oscillating modulation scheme could be chosen, but the variation in the switching frequency associated with self-oscillating modulations has to be taken into account. This is the subject treated by paper A.6, which will be reviewed next. The complete NSE will be the subject of section 4.3.

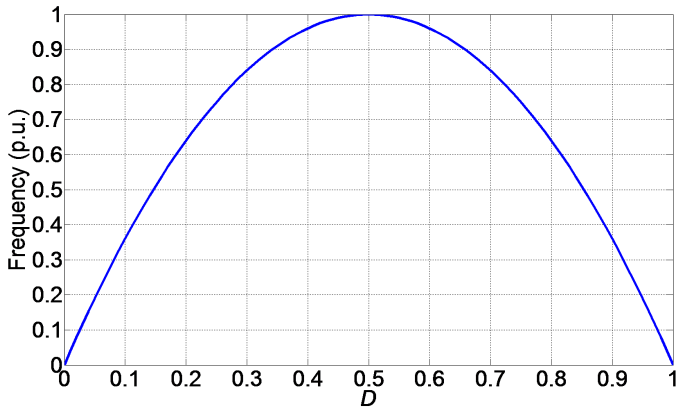


Figure 4.1: Frequency (normalized to the maximum frequency) versus changes of duty cycle of a hysteresis self-oscillating modulator.

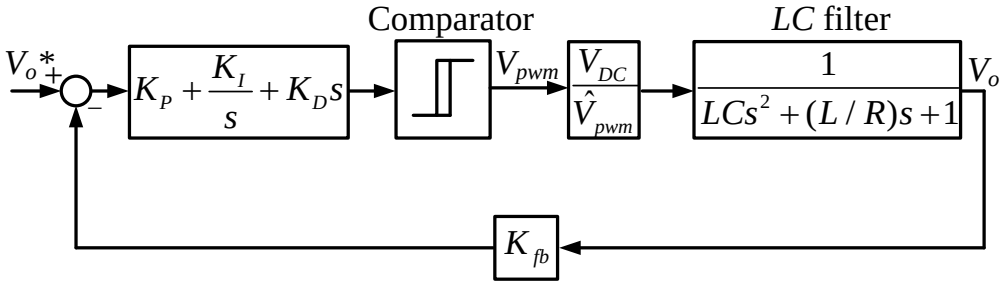


Figure 4.2: A global loop integrating modulator controller (GLIM– [4]).

4.2 Constant switching frequency self-oscillating control scheme

A review of different existing methods for fixing the switching frequency of a self-oscillating controlled system can be found in paper A.6. It is not restated here.

4.2.1 Proposed method

This section will summarize the solution discussed in paper A.6 entitled "Constant Switching Frequency Self-Oscillating Controlled Class-D Amplifiers." The study and its discussions are for a class-D amplifier (a second-order output filter synchronous buck converter), but the proposed method is applicable to any converters which utilize a hysteresis modulation scheme, such as the buck converter with higher-order output filters, the boost converter, the ac-dc rectifier, the ac-ac converter, the dc-ac inverter, etc.

Fig. 4.2 shows a typical hysteresis-based, self-oscillating control system for class-D amplifiers. This scheme is usually referred to as the Global Loop Integrating Modulator (GLIM) [4]. Despite producing excellent audio performance (very low THD/SNR) around idle mode, the uncompensated scheme suffers from a large variation of switching frequency when the duty cycle is moving towards the too

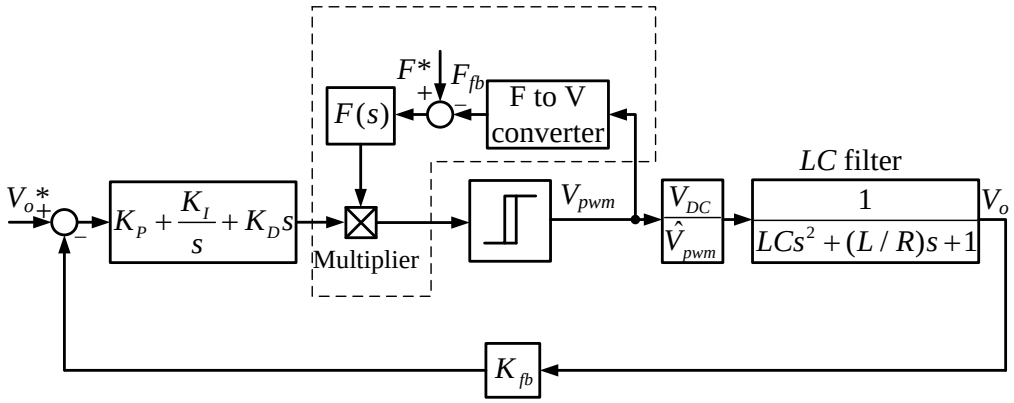


Figure 4.3: The proposed fixed frequency self-oscillating modulation scheme.

limit (0 and 1).

Fig. 4.3 demonstrates the application of the proposed fixed *f*requency *s*elf-*o*scillating *m*odulation *s*cheme (FSOMS) to a synchronous buck converter with a 2^{nd} order output filter. The proposed FSOMS is inside the dashed box.

The PWM signal generated by the hysteresis comparator is converted to a voltage proportional to its frequency. This is done by passing the PWM to a mono-stable multi-vibrator (MMV) or one-shot circuit with a fixed pulse width output. Each time the input to the MMV has a rising edge, the output of the MMV generates a pulse with a fixed width, which is 100 ns in this case. The resulting signal of the MMV is low-pass filtered by a first order *RC* filter circuit. Only the dc value of the MMV remains, and it is proportional to the switching frequency. The operation of the MMV and the F-to-V converter are illustrated in Fig.4.4 and Fig. 4.5. The measured switching frequency is compared to the reference switching frequency and processed by a compensator $F(s)$. $F(s)$ can be implemented with a PI (proportional-integral) or PID (proportional-integral-derivative) controller. The output of $F(s)$ is the compensating gain for the self-oscillating control loop, and it is inserted to the control loop through a multiplier. It adjusts the switching frequency of the converter to track the reference frequency, which is represented by F^* on Fig. 4.3

4.2.2 Verifications

The simulation studies examine different responses of the converter using the self-oscillating control approach without frequency compensation as well as with the proposed frequency compensation. The responses are based on both dc reference signals and sinusoidal audio reference signals. Simulation model was built in MATLAB/Simulink environment. Most parts of the controllers and feedback were modelled and simulated by realistic commercially available discrete components: non-ideal operational amplifiers with limited gain-bandwidth product and limited output voltage ability, etc.

Fig. 4.6 shows the voltage transient (step) response of the converter without a frequency compensator and with the proposed frequency compensator. The dc reference values are swept so that the duty cycle of the output voltage is changed.

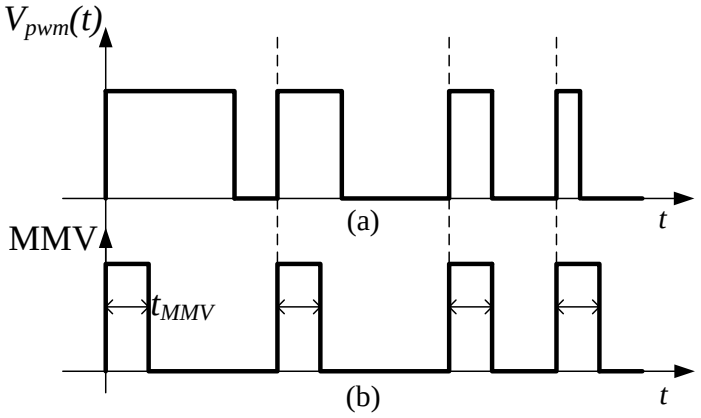


Figure 4.4: Operation of the MMV a) the PWM output signal of the comparator, b) the output signal of the mono-stable multi-vibrator.

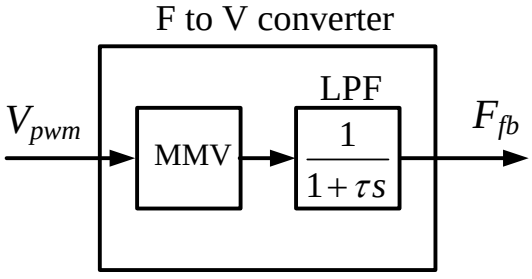
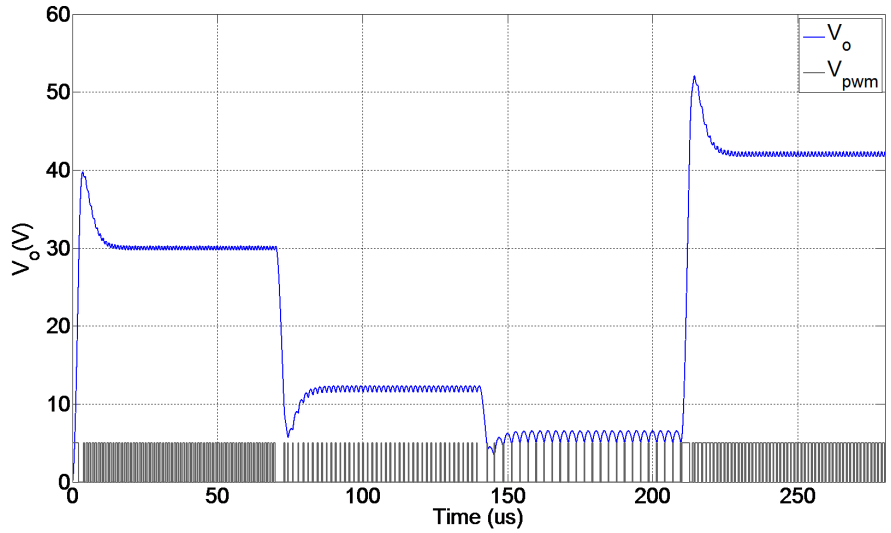
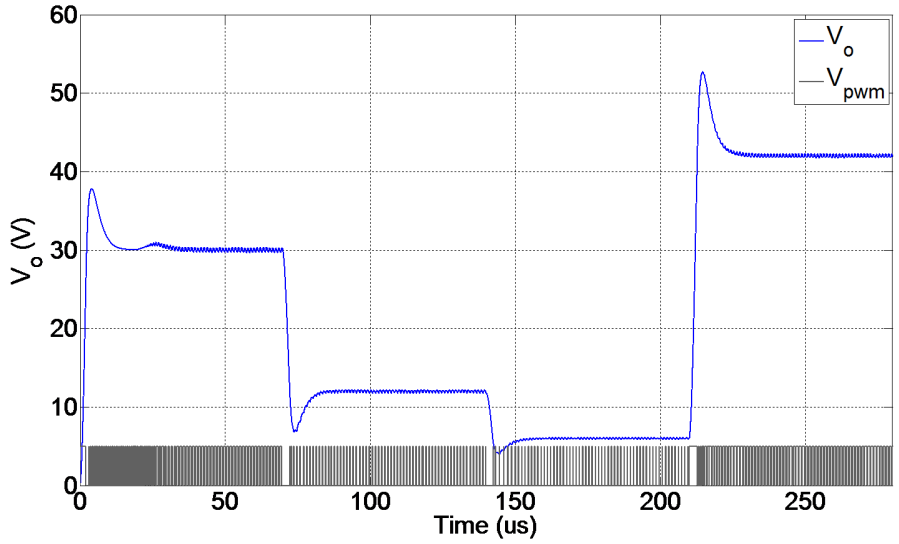


Figure 4.5: Frequency to voltage (F to V) converter.

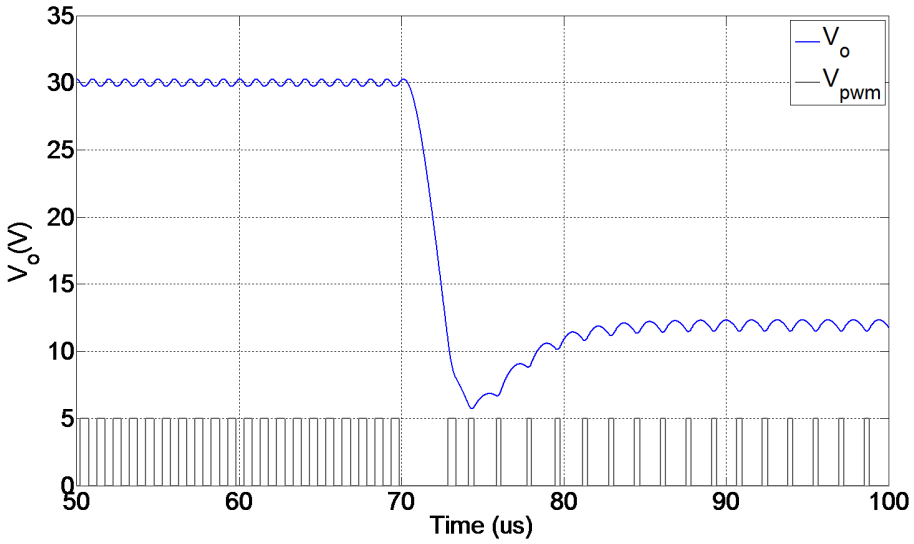


(a)

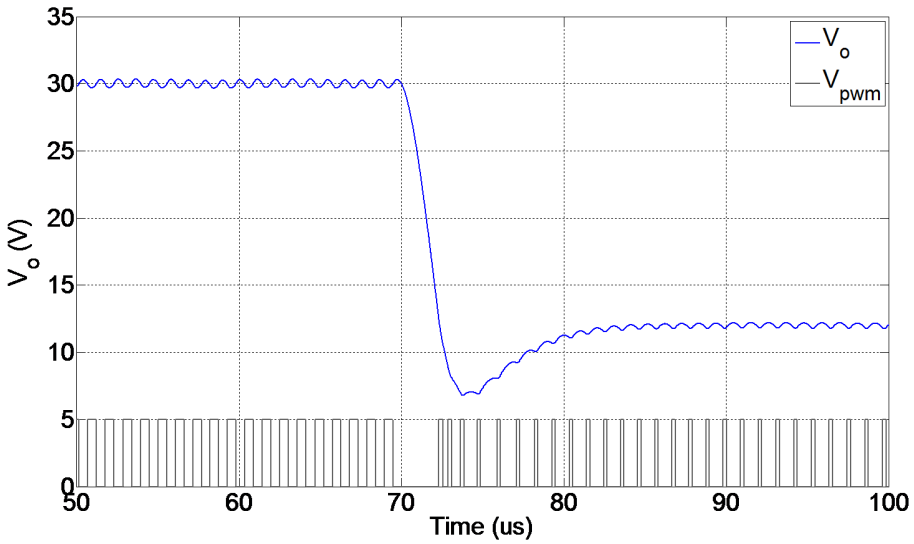


(b)

Figure 4.6: Step response of output: a) without a frequency compensator, b) with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is swept from 0.5 to 0.2, 0.1, and 0.7.

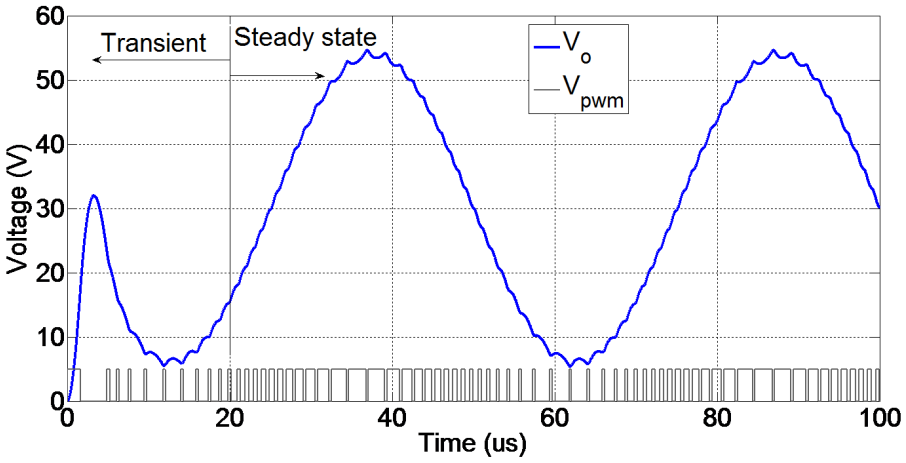


(a)

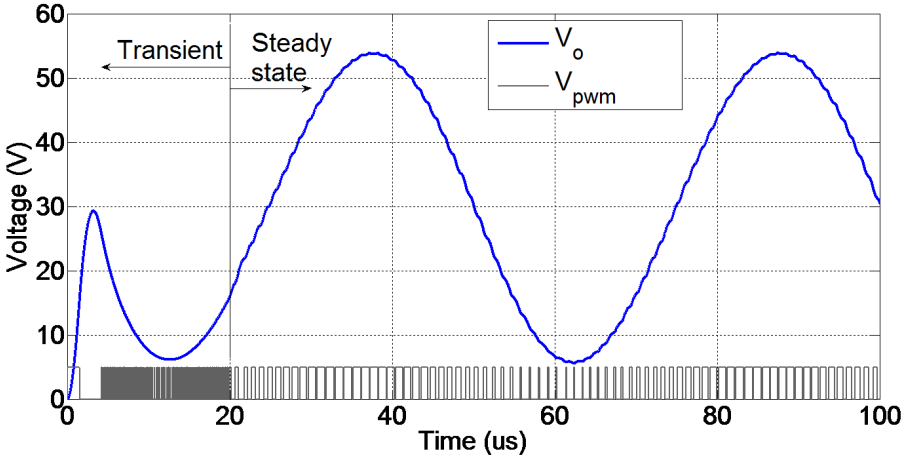


(b)

Figure 4.7: Partial zoom of the step response of output voltage: a) without a frequency compensator, b) with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm}(V), the duty cycle is shifting from 0.5 to 0.2 at time 70 μs.



(a)



(b)

Figure 4.8: Output response to a 20 kHz audio reference: a) without a frequency compensator, b) with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is continuously varying from 0.1 to 0.9 and vice versa.

At time t = 0, the duty cycle is 0.5. At times t = 70 μs, t = 140 μs, and t = 210 μs, the duty cycle is 0.2, 0.1, and 0.7, respectively. The bottom of Fig. 4.6a shows the switching signal generated by the comparator. It can be seen that the switching frequency varies with the change of the duty cycle. Its peak value is at the centre frequency where $D = 0.5$. This phenomenon can be observed more clearly from a partial zoom of Fig. 4.6a which is shown in Fig. 4.7a. As can be seen from Fig. 4.6b and Fig. 4.7b, with the proposed frequency compensator, the switching frequency of the converter in steady state held constant regardless of the variation in the output voltage or duty cycle. The steady-state response of the output voltage has been improved, while a desirable transient response is preserved. The ripple of the output voltage is reduced at all switching duty cycles that are different from the 0.5 duty cycle.

Fig. 4.8 shows responses to an audio signal of the conventional converter without and with the frequency compensator. The frequency of the signal is 20 kHz, which represents an audio signal for typical human hearing ability. It can be confirmed again from the simulation result of Fig. 4.8a, that the switching frequency varies with the magnitude of the audio signal, or in other words, it varies with the switching duty cycle. As Fig. 4.1 suggests, the drop of the frequency at higher modulation index creates larger output ripple and distortion. This phenomenon can be observed from the top and bottom of the output voltage signal of Fig. 4.8a. On the contrary, with the proposed frequency compensator, the switching frequency of the converter has been held constant even with a large variation in the duty cycle over one period. This can be observed from Fig. 4.8b. The ripple at the top peak and bottom peak of the output signal, therefore, has been significantly improved compared to Fig. 4.8a. The amplifier with the proposed constant-frequency compensator outperforms the traditional one without a frequency compensator.

To compare different methods with each other, different simulations are performed at various duty cycles. The nominal frequency used in the test is 1 MHz. The switching frequencies are plotted in Fig. 4.9 for four cases: calculated by equation 4.3, simulated model without a frequency compensator, simulated model with the proposed frequency compensator, and simulated model with method proposed in [5]. As can be seen, the simulated switching frequency without a frequency compensator matches well with the calculation. Moreover, a constant switching frequency is guaranteed with the method proposed in this work.

From the control block diagram of the proposed circuit, all control parts can be realized by standard analog circuit consisting of operational amplifiers, comparators, and *RC* network, except for the multiplier. It is suggested that the multiplier unit be an analog multiplier IC for its fast response.

4.3 High dynamic performance nonlinear source emulator

This section is the highlight of the thesis. It summarizes the discussion reported in paper A.7. [65].

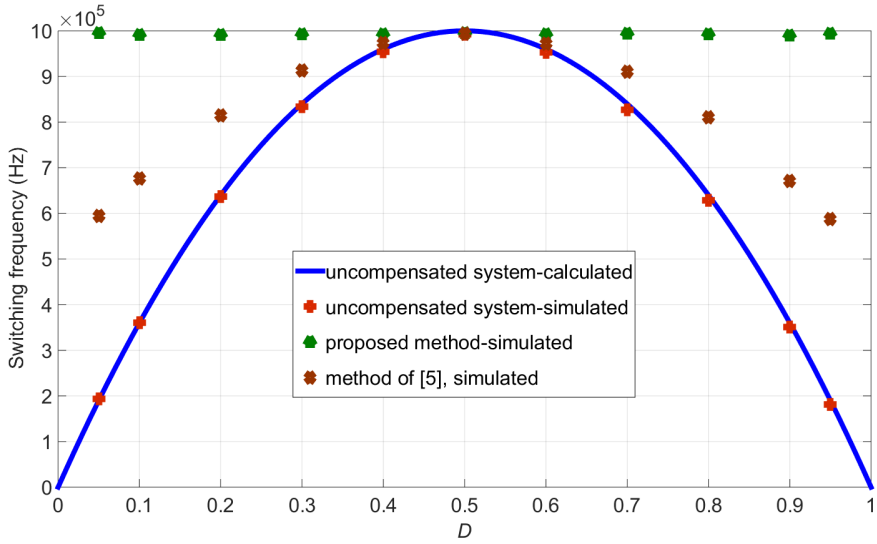


Figure 4.9: Switching frequency versus variation of duty cycle: calculated results without frequency compensation, simulated results without frequency compensation, simulated results with the proposed frequency compensation, and simulated results with the method proposed in [5].

4.3.1 Circuit design

The proposed NSE consists of a voltage-controlled tracking converter (VCTC) and a nonlinear curve reference generator (NCRG).

In Fig. 4.10, the steady state operation and the gradient of the current-voltage (I-V) curve is determined by three parameters. The short circuit current is determined by the value of I_{SC}; in this prototype, I_{SC} is converted to a voltage signal with (1 A/1 V) conversion. The parallel resistor which determines the gradient (or the slope) of the I-V curve around the constant current region, is represented by R_P. The open circuit voltage is controlled by the ratio k_V/R_I. Changing the ratio k_V/R_I will change the open circuit voltage of the proposed NSE.

The NCRG in the bottom of Fig. 4.10 consists of summation circuits and a voltage to current (V2I) converter. The V2I consists of *pnp* transistors Q_3 and operational amplifier OA2. V_{CC} is the 12 V control supply for all the operational amplifiers. The negative control supply, $-V_{CC} = -12$ V, is applied to the cathode of diode D in order to ensure proper operation for the V2I converter. As can be seen from Fig. 2.3, the current flows through the diode is equal to the difference between the short circuit current and the output current. Using the proposed circuit, the voltage signal which is the difference between I_{SC} and I_o (in volt), is converted to current I_D (in ampere) by:

$$I_D = \frac{V_{I_{SC}} - V_{I_o}}{R_I} \text{ (A)}. \tag{4.4}$$

Thus, the voltage-drop accross diode D and R_P will be the signal level NSE output

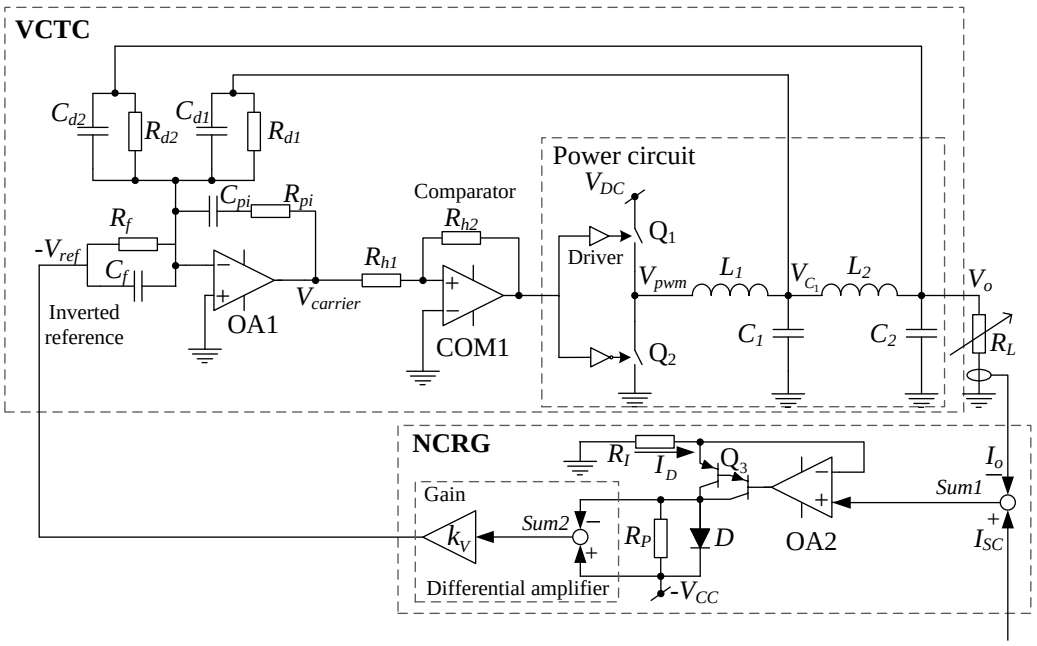


Figure 4.10: The schematic of the proposed nonlinear source emulator.

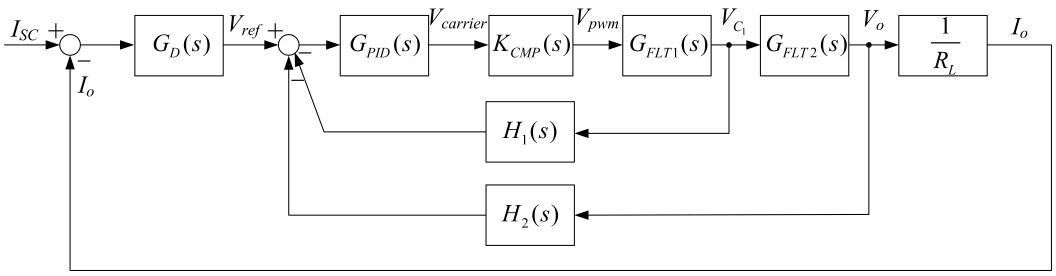


Figure 4.11: The block diagram of the control transfer functions.

voltage. A differential amplifier takes the voltage accross D and scales it with k_V. The resulting voltage, $-V_{ref}$, will be the reference voltage for the tracking converter.

The output voltage of a nonlinear source such as fuel cell or PV system is usually ripple-free so the output of the NSE should have a ripple which is as low as possible. For this reason, a fourth order output filter is utilized at the output of the tracking converter instead of a second order output filter because of its possible higher attenuation at a given switching frequency. The output filter transfer function, which is from the pulse power signal, V_{pwm}, to the output voltage, V_o, is approximated at high frequency by:

$$G_{FLT}(s)_{(s\gg max(j\omega_1,j\omega_2))} = \frac{V_o(s)}{V_{pwm}(s)}_{(s\gg max(j\omega_1,j\omega_2))} \approx \frac{1}{s^4 L_1 L_2 C_1 C_2} = \frac{\omega_1^2\omega_2^2}{s^4}, \tag{4.5}$$

where $\omega_1 = \frac{1}{\sqrt{L_1 C_1}}$ and $\omega_2 = \frac{1}{\sqrt{L_2 C_2}}$ are the natural frequency of each filter stage.

At the switching frequency ω_{sw} (rad/s), the magnitude of the output filter is:

$$|G_{FLT}(j\omega_{sw})| \approx \frac{\omega_1^2\omega_2^2}{\omega_{sw}^4}. \tag{4.6}$$

With the filter value provided in Table 4.1 and with a switching frequency of 1 MHz, from (4.6), the fundamental harmonic at the output of the tracking converter will have a magnitude of approximately 35 mV peak to peak.

The modelling of the tracking converter is as follows. $G_D(s)$ is the transfer function from the different between the short circuit current I_{SC} and the output current I_o to the reference voltage V_{ref}:

$$G_D(s) = \frac{V_{ref}(s)}{I_{SC}(s) - I_o(s)} = \frac{k_V Z_D R_P}{R_I(Z_D + R_P)}, \tag{4.7}$$

where Z_D is the impedance of the diode D used. $G_D(s)$ is small when the circuit operates near the open circuit region, and it increases when the operating point move towards the short circuit.

The transfer function of the PID controller as shown is:

$$G_{PID}(s) = \frac{(R_{pi}C_{pi}s + 1)(R_f C_f s + 1)}{C_{pi}R_f s}. \tag{4.8}$$

$K_{CMP}(s)$ is the transfer function from the output of the PID controller to the pulse power signal V_{pwm}. A detail treatment of $K_{CMP}(s)$ can be found in, for example, [66]. Reference [63; 67] approximated $K_{CMP}(s)$ to be an infinite gain and achieved reasonable results. For simplicity, in this work, K_{CMP} is simplified to be a dc gain which is:

$$K_{CMP}(s) = \frac{V_{pwm}(s)}{V_{carrier}(s)} \approx \frac{V_{DC}}{\varepsilon} = \frac{V_{DC}R_{h2}}{V_{CMP}R_{h1}}, \tag{4.9}$$

where $\varepsilon = \frac{V_{CMP}R_{h1}}{R_{h2}}$ is the hysteresis threshold, V_{CMP} is the output of the comparator COM1.

$G_{FLT1}(s)$ is the transfer function from V_{pwm} to V_{C_1}, which is (by [63]):

$$G_{FLT1}(s) = \frac{s^2L_2C_2 + sL_2/R_L + 1}{s^4L_1L_2C_1C_2 + s^3\frac{L_1L_2C_1}{R_L} + s^2(L_1C_2 + L_1C_1 + L_2C_2) + s\frac{L_1+L_2}{R_L} + 1}. \tag{4.10}$$

$G_{FLT2}(s)$ is the transfer function from V_{C_1} to V_o, which is:

$$G_{FLT2}(s) = \frac{V_o(s)}{V_{C_1}(s)} = \frac{1}{s^2L_2C_2 + sL_2/R_L + 1}. \tag{4.11}$$

The most inner feedback transfer function is:

$$H_1(s) = \frac{R_f(R_{d1}C_{d1}s + 1)}{R_{d1}(R_fC_fs + 1)}. \tag{4.12}$$

Likewise, the output-voltage feedback transfer function is:

$$H_2(s) = \frac{R_f(R_{d2}C_{d2}s + 1)}{R_{d2}(R_fC_fs + 1)}. \tag{4.13}$$

The most inner loop closed loop transfer function is:

$$G_{IN-CL}(s) = \frac{V_{C_1}(s)}{V_{ref}(s) - V_o(s)H_2(s)} = \frac{G_{PID}(s)K_{CMP}(s)G_{FLT1}(s)}{1 + G_{PID}(s)K_{CMP}(s)G_{FLT1}(s)H_1(s)}. \tag{4.14}$$

Since $K_{CMP}(s)$ is a very high gain, $G_{IN-CL}(s)$ can be approximated to be:

$$G_{IN-CL}(s) \approx \frac{1}{H_1(s)} \tag{4.15}$$

Transfer function from reference voltage to the output voltage is then:

$$G_V(s) = \frac{V_o(s)}{V_{ref}(s)} = \frac{G_{IN-CL}(s)G_{FLT2}(s)}{1 + G_{IN-CL}(s)G_{FLT2}(s)H_2(s)} \tag{4.16}$$

$$\approx \frac{G_{FLT2}(s)}{H_1(s) + G_{FLT2}(s)H_2(s)}. \tag{4.17}$$

A Bode plot of $G_V(s)$ based on (4.16) and the parameters in Table 4.1 is shown in Fig. 4.12 for different loads.

The dc gain of the closed loop of the voltage is:

$$G_V(0) = \frac{R_{d1}R_{d2}}{R_f(R_{d1} + R_{d2})}. \tag{4.18}$$

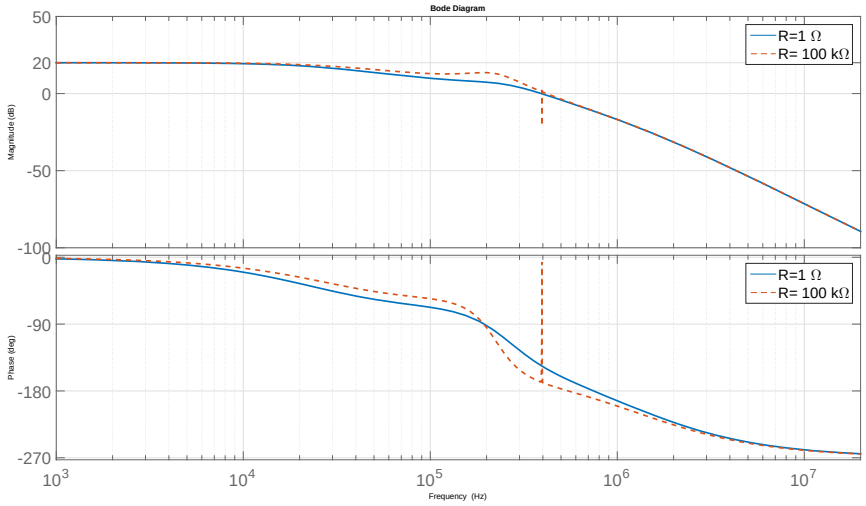


Figure 4.12: Bode plot of the closed voltage loop at different loads.

Table 4.1: Parameters of the tracking converter and its control

L_1	3.3 μH	C_f	1 nF
L_2	3.3 μH	R_{d1}	20 kΩ
C_1	100 nF	C_{d1}	47 pF
C_2	1360 nF	R_{d2}	20 kΩ
V_{DC}	60 V	C_{d2}	470 pF
R_{h1}	6.2 kΩ	R_{pi}	1 kΩ
R_{h2}	51 kΩ	C_{pi}	470 pF
R_f	1 kΩ	V_{CMP}	5 V
A_V	10		

4.3.2 Experimental results

The experimental studies have examined the proposed NSE under four typical operating conditions usually faced by a state-of-the-art nonlinear source. They are the steady state response along the static I-V curve, the load step between nominal and open circuit, the load step between nominal and short circuit, and the step change of input sources. In addition, the fifth test is also added, which is a *fictitious* step change of temperature. The fifth test is fictitious because a step change of temperature is physically unrealizable because of the thermal inertia of the nonlinear source material. For example, after a sudden change of irradiation, a PV panel will usually takes approximately 30 minutes to reach its steady state temperature [68]. Although a step change of temperature is unlikely, it will be still tested here in order to verify the dynamic capability of the proposed NSE.

A photo of the prototype can be found in Fig. 4.13.

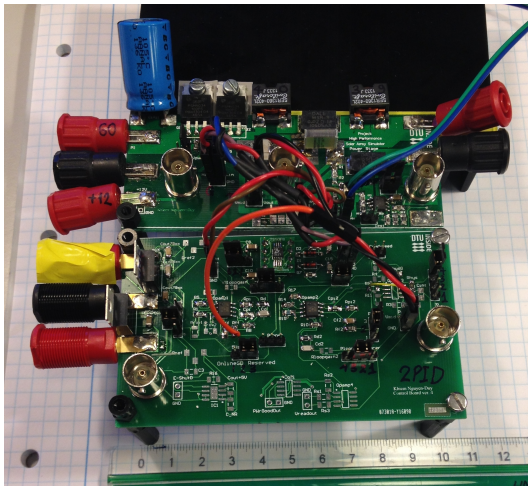


Figure 4.13: A photo of the prototype.

4.3.2.1 Static I-V curve

Figs. 4.14 and 4.15 show the steady state current-voltage (I-V) and power-voltage (P-V) curves generated by the prototype with the set up in Table 4.2. As can be seen, the output voltage and current resemble the output of a nonlinear source such as of a fuel cell, battery, or PV panel. The MPP with this set up is 131 W at a load impedance of approximately 10 Ω.

4.3.2.2 Load step between nominal and open circuit

The load step between nominal and open circuit or i.e., series-type switching regulation configuration, is shown in Fig. 4.16. Meanwhile, Fig. 4.17 shows the transient responses of the proposed NSE under this regulation. The load is switching between two values: open circuit (where the load is infinitive) and a fixed load. The switching frequency of the load is about 1 kHz. As can be seen, the output voltage and current finish each transient within 10 μs. It is interesting to observed the

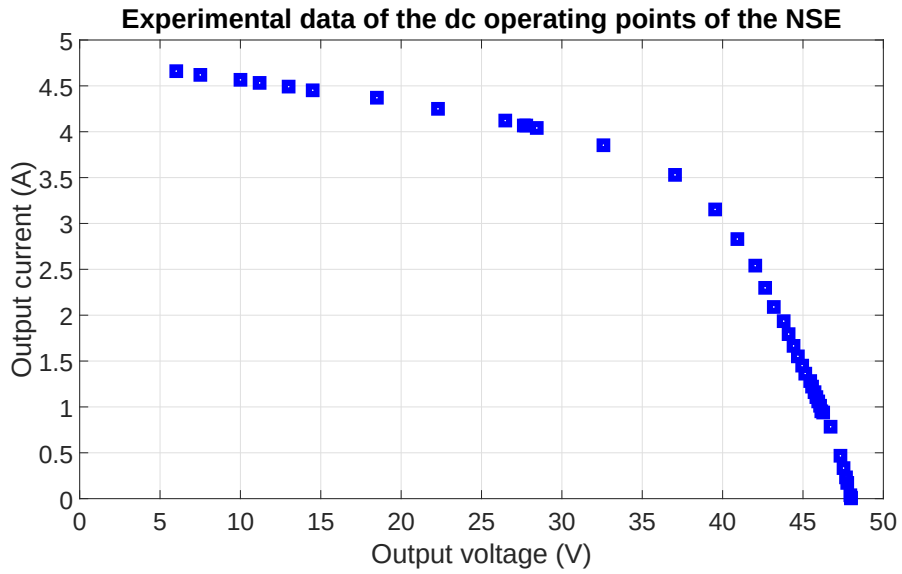


Figure 4.14: The static current-voltage (I-V) curve generated by the proposed NSE.

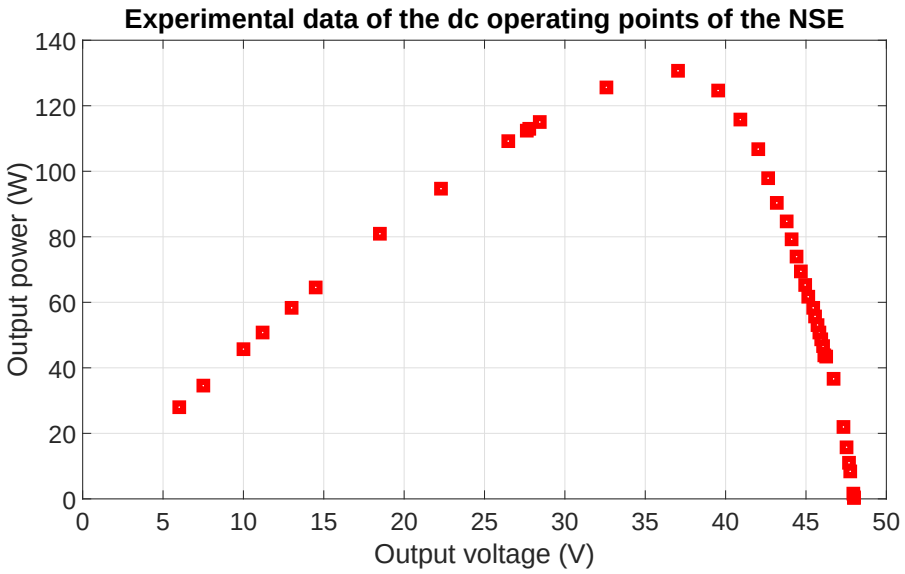


Figure 4.15: The static power-voltage (P-V) curve generated by the proposed NSE.

Table 4.2: Parameters used to generate static I-V curve

Parameter	Value
I_{SC}	5 V (5 A)
R_P	10 Ω
R_I	15 Ω
k_V	5
V_{OC}	48 V

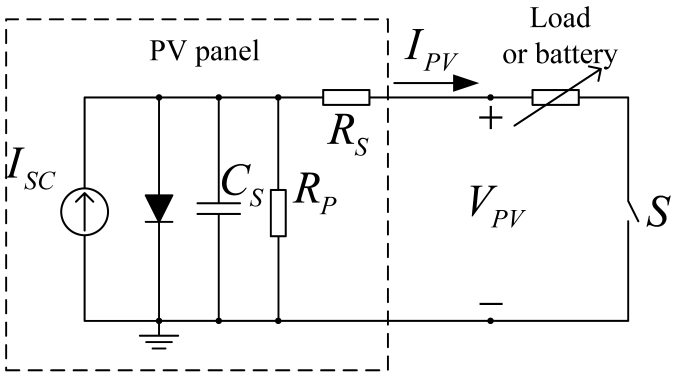


Figure 4.16: Circuit configuration of load step between nominal and open circuit or a series-type switching voltage regulator

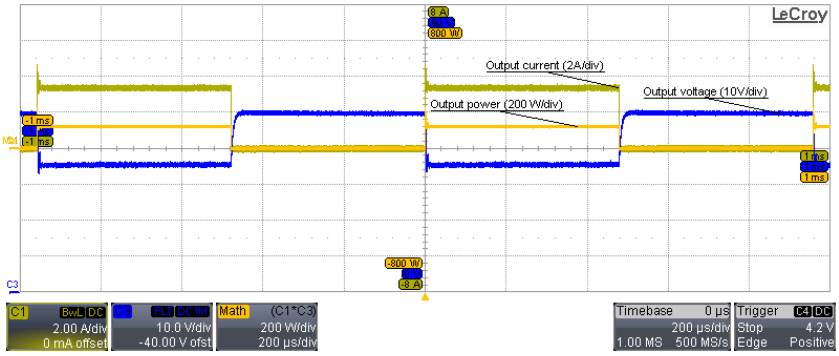
experimental I-V curve of this test recorded directly from the oscilloscope used in the tests, which can be referred to Fig. 4.18a. Meanwhile, Fig. 4.18b explains the process of Fig. 4.18a, which will be as follows. The NSE is switching between point A and B of Fig. 4.18b. Right after the fixed load is inserted to the output of NSE, the circuit immediately moves from point A to A1. During this period, the voltage does not change yet due to its disturbance rejection capability, while the new current becomes voltage at A divided by the fixed load. After that, the regulation of the NSE makes the circuit moves from A1 to B and the whole process from A to B takes only 10 μs (see Fig. 4.17c). From now, the circuit settles at B until the load is changed. Likewise, when the load is switched from the fixed load to open circuit, which is from B to A, it will first move immediately to B1, then move from B1 to A. The whole transition from B to A takes 10 μs, which can be verified from Fig. 4.17b.

4.3.2.3 Load step between nominal and short circuit

The load step between nominal and short circuit configuration is shown in Fig. 4.19.

The prosed circuit, unfortunately, suffers from instability at short circuit current. According to [34], this is a typical characteristic of the voltage-control approach. Also according to [34], the current control approach does not have similar problem in the short circuit region, but it suffers from poor controllability and stability near the open circuit region.

The instability of the proposed NSE at operating points close to the short circuit can be explained as follows. Near the short circuit region of the I-V curve, the load impedance R_L is small in Ohmic value, making the gain from V_o to I_o become large compared to that in other region. In addition, the output current is approaching I_{SC}, which will make I_D approach zero. This small current makes the impedance of diode D approach infinitive according to the diode I-V curve. This makes $G_D(s)$ becomes very large. The open loop gain consists of $G_D(s), G_V(s)$, and $\frac{1}{R_L}$ becomes very large. Its cross-over frequency will be moved towards the high frequency, where the phase margin becomes negative (see Fig. 4.12) which makes the system unstable.



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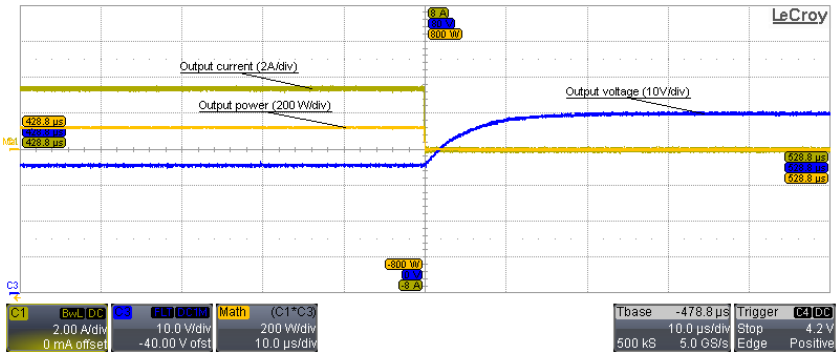
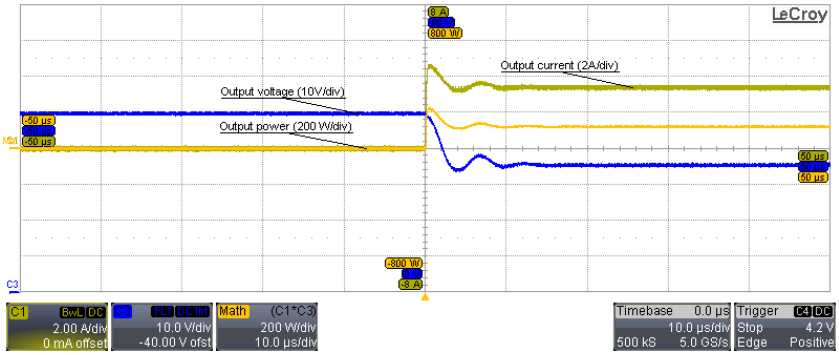
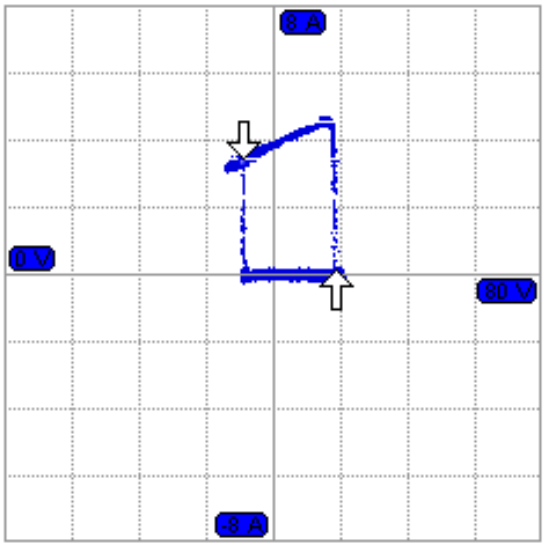


(b)

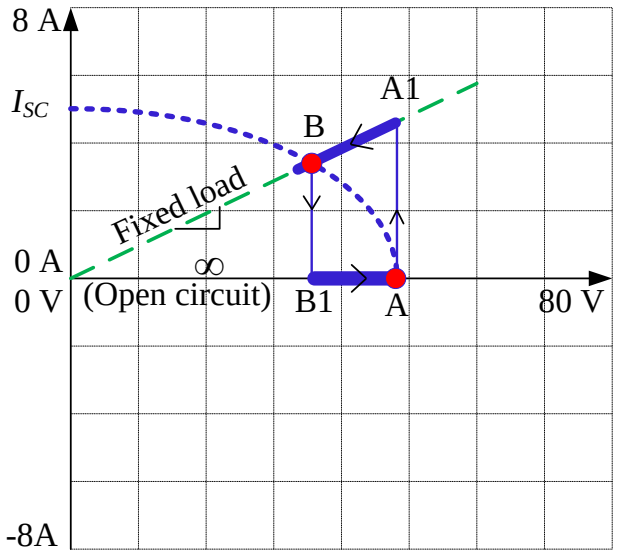


(c)

Figure 4.17: Series-type switching regulation test (a) switching transient between open circuit and a fixed load (b) partial zoom of the circuit transients from fixed load to open circuit (c)partial zoom of the circuit transients from open circuit to a fixed load. Channel 1 (olive color): output current, 2 A/div. Channel 3 (blue color): output voltage, 10 V/div. Channel Math (C1*C3) (orange color): output power, 200 W/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.



(a)



(b)

Figure 4.18: Series-type switching regulation test. (a) Experimental I-V curve and (b) its analytical waveform.

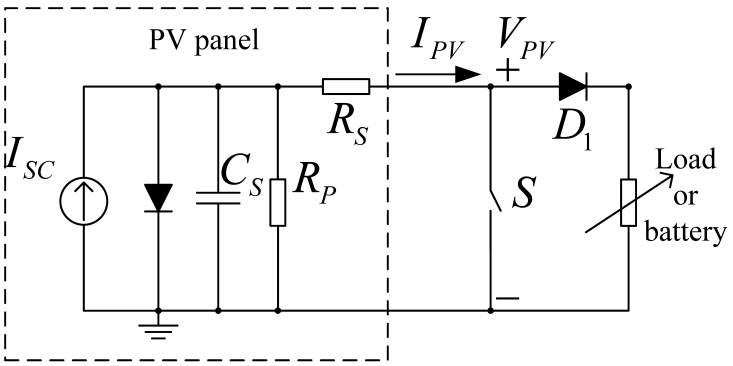


Figure 4.19: Circuit configuration of a load step between nominal and short circuit.

The load step between nominal and short circuit problem of voltage-controlled NSEs will not be addressed in this thesis; it may the treated in a separate future work.

4.3.2.4 Step change of input source

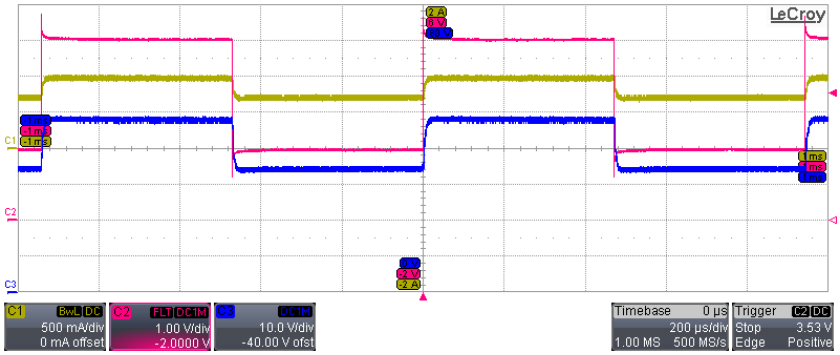
The input source of a nonlinear source can be fuel, wind, irradiation, etc. The results of the step change of an input source which can happen in a nonlinear source are shown in Figs. 4.20 and 4.21. In Fig. 4.20, channel 2 (red color) is the short circuit current I_{SC}. The input source change causes a change of short circuit current from 2 A to 5 A and vice versa. From Figs. 4.20b and 4.20c, the circuit only takes 10 μs to complete the transition. The experimental I-V curve is shown in Fig. 4.21a and its behavior is explained in Fig. 4.21b. A reduction of the input source level from 5 A to 2 A short circuit current will make the NSE move from point A to B, and an increase of the input source in the other direction will make the NSE move from point B to A. Each transition takes 10 μs.

4.3.2.5 Step change of temperature tests

As discussed in the previous Section, the open circuit voltage is determined by the ratio of k_V to R_I. The fictitious step change of temperature can be simulated by switching between different value of R_I. To demonstrate this, a value of 15 Ω and 30 Ω are switched. The results are shown in Figs. 4.22 and 4.23. The short circuit current is fixed at 5 A. When changing the temperature, the short circuit current does not change, but the profile of I-V curve changes as shown in Fig. 4.23b. As can be seen from these results, under a step change of temperature, the proposed NSE only takes about 10 μs to complete a transition.

4.3.3 A proposed current controlled NSE

It is worth studying the current controlled approach shown in Fig. 2.5. In this work, a possible current controlled NSE is proposed in Fig. 4.24. The current controlled NSE consists of a current controlled tracking converter (CCTC) and a nonlinear



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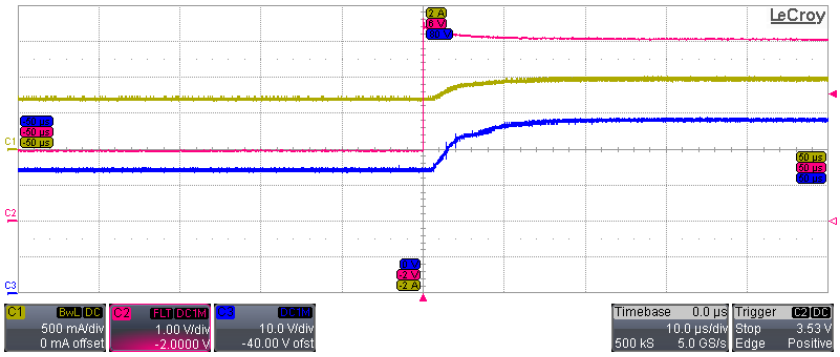

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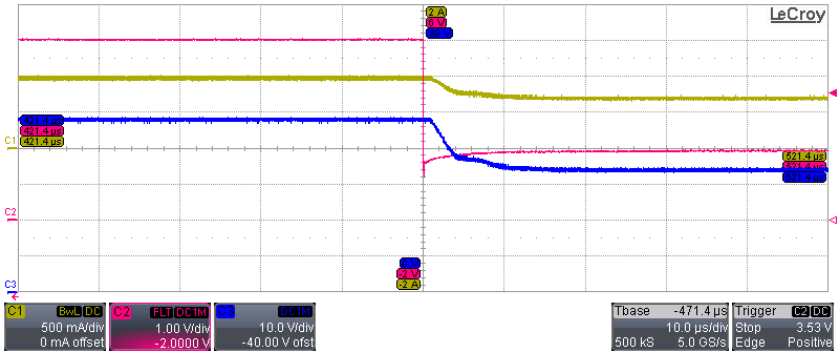
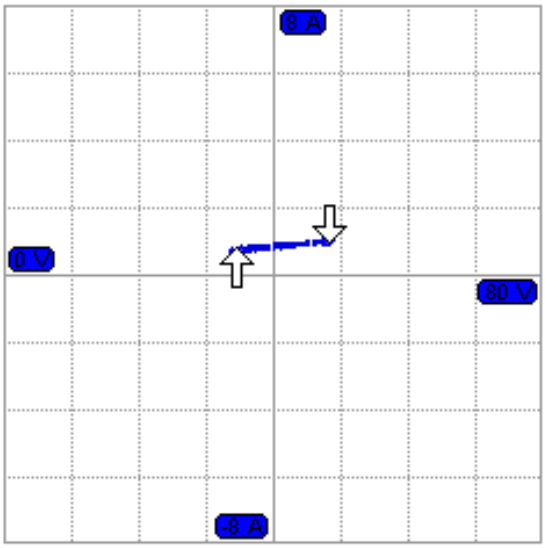
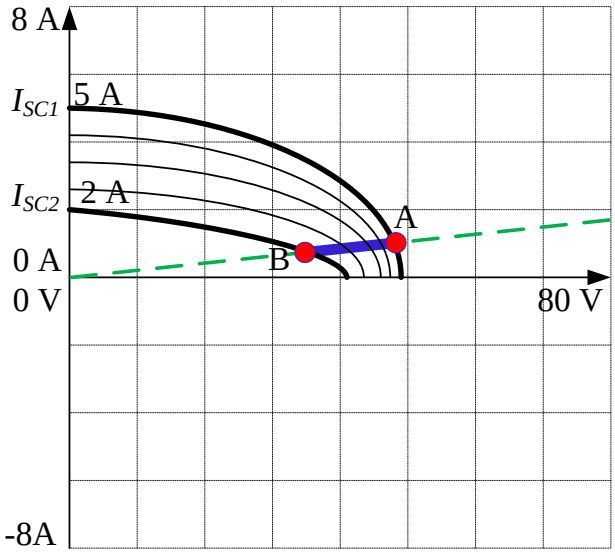


(c)

Figure 4.20: Emulation of input source step change (a) switching transient between two input source levels (b) partial zoom of the transients from a low to high input source level (c) partial zoom of the transients from a high to low input source level. Channel 1 (olive color): output current, 2 A/div. Channel 3 (blue color): output voltage, 10 V/div. Channel 2 (red color): input source level, 1 A/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.

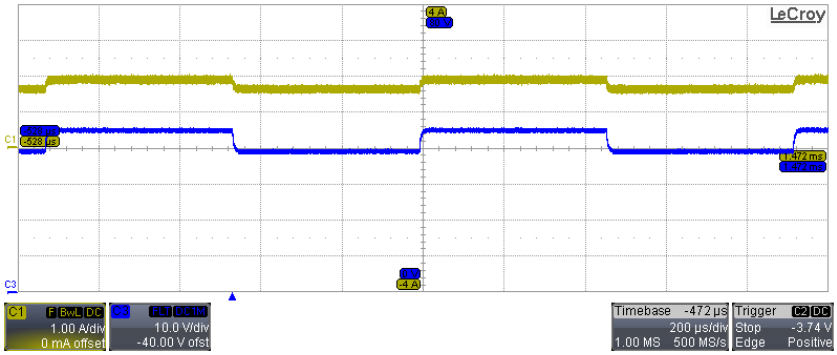


(a)

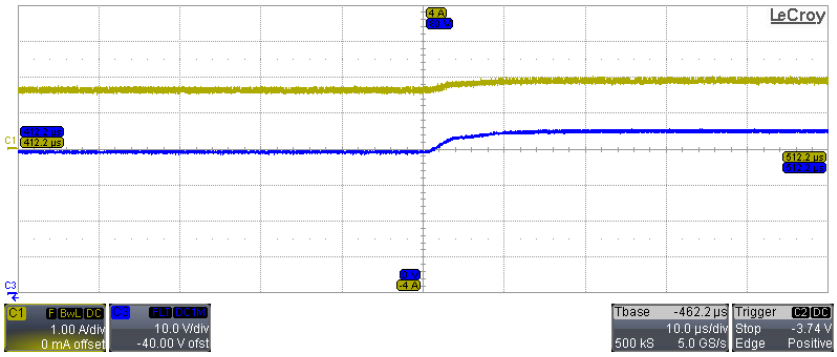


(b)

Figure 4.21: Step change of input source. (a) Experimental I-V curve and (b) its analytical waveform.



(a)



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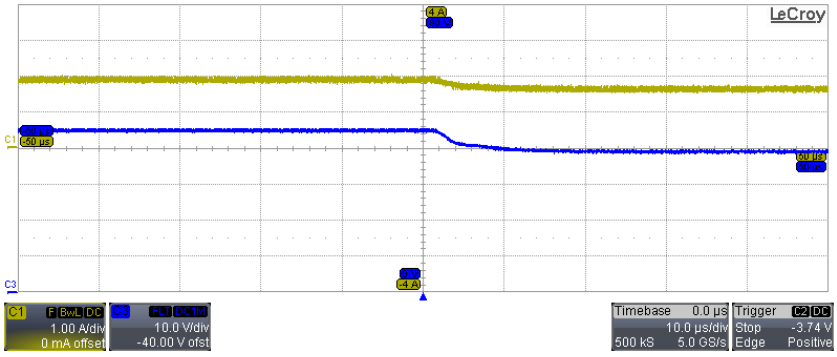
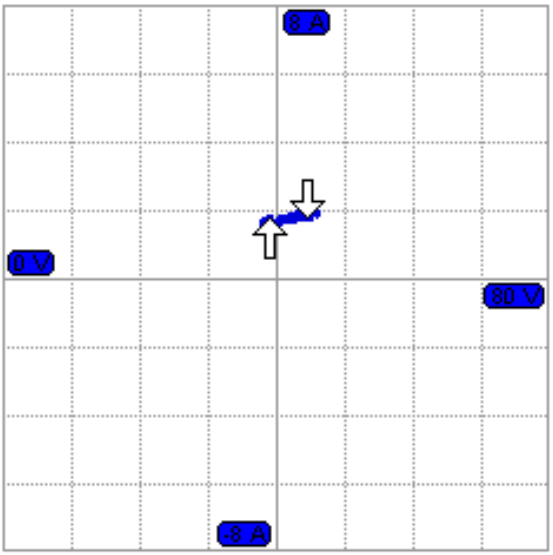
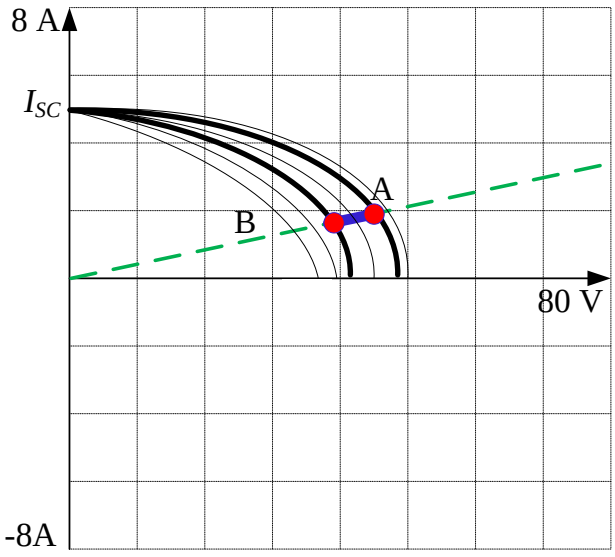


(c)

Figure 4.22: Emulation of fictitious temperature step change (a) switching transient between two temperature levels (b) partial zoom of the transients from a low to high temperature level (c) partial zoom of the transients from a high to low temperature level. Channel 1 (olive color): output current, 1 A/div. Channel 3 (blue color): output voltage, 10 V/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.



(a)



(b)

Figure 4.23: Fictitious temperature step change effect. (a) Experimental I-V curve and (b) its analytical waveform.

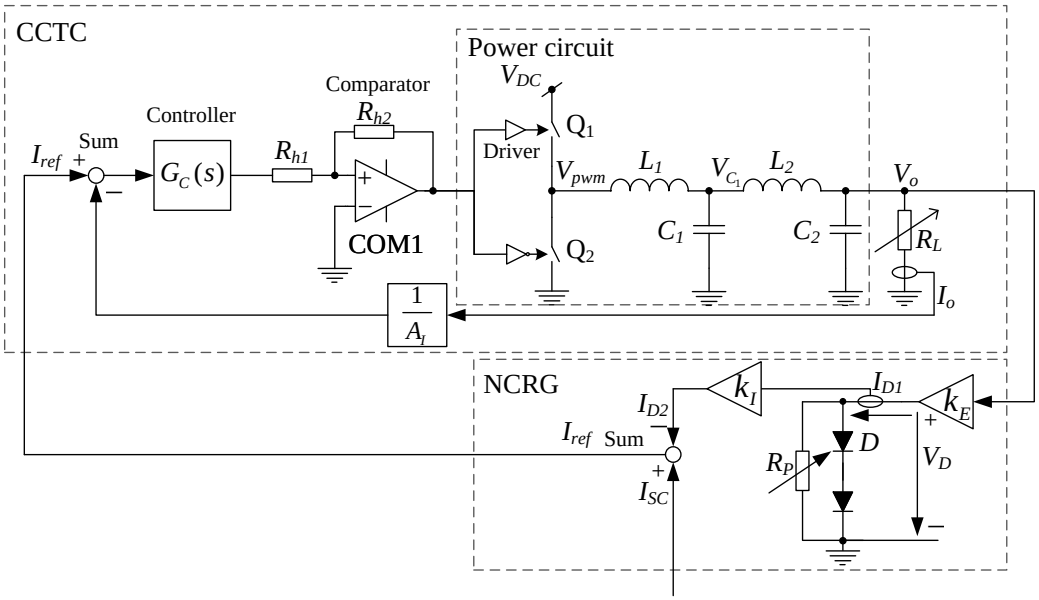


Figure 4.24: A proposed current controlled nonlinear source emulator.

curve reference generator (NCRG). The output voltage is fed back to the NCRG and the NCRG generates the reference output current I_{ref}. The output current I_o is sensed and conditioned by a gain $\frac{1}{A_I}$ and compared to the reference current. $G_C(s)$ is the controller (compensator) of the current loop, ensuring a zero steady state error. In steady state, $I_o = A_I I_{ref}$.

The NCRG can be implemented by either a digital circuit by means of a look-up table or mathematics calculation. In the proposed analogue NCRG, the voltage is scaled down by a voltage divider, which represented by gain k_E. The resulting voltage V_D is buffered and applied to a diode circuit consist of diode D and parallel resistor R_P. Current I_{D1} flowing through the diode circuit is scaled by a gain k_I and then subtracted by the reference short circuit current I_{SC}. The result is the reference signal, I_{ref}.

The short circuit current is determined by the external signal I_{SC}. The open circuit voltage is determined by the gain $k_E k_I$.

The proposed circuit has been successfully verified by LTSpice simulation environment. Unfortunately, due to limited time, the circuit was not realized into hardware and therefore, it could be a subject of future work.

Chapter 5

Conclusion and future work

5.1 Conclusion

This thesis has studied and developed a NSE system suitable for the testing of different nonlinear sources. The proposed solution consists of an ultra low circuit input-to-output capacitance (C_{io}) power supply and an NSE. The results that have been achieved are a C_{io} of 10 pF in a 300-W power supply prototype and a 200-W NSE capable of simulating series-type switching tests and step change of input source tests with the fastest transient response ever reported, 10 μs. In addition, the achieved capacitance per output power is 0.033 pF/W, which is 30 times lower than the typical 1 pF/W of existing approaches.

Furthermore, the modular approach proposed by this work will allow for flexible stacking or paralleling of multiple modules in order to satisfy custom power rating. This work, therefore, has provided a complete solution for simulating a group of nonlinear sources with different working conditions.

Important results have been provided along with the thesis or referred to relevant publications resulting from this work. Some of the key results from this work can be selected and summarized as follows.

For the isolated power supply:

1. The interwinding capacitance of the transformer predominates the power supply C_{io}. The interwinding capacitance should be minimized, especially if the loads of the power supply exhibit high dv/dt at their outputs.

2. Feedbacks from one side to the other of an ultra-low C_{io} power supply should be avoided if possible. Otherwise, the feedback will add to the overall C_{io}.

3. Leakage inductance and interwinding capacitance are opposite in magnitude to each other. A power converter designed with very low transformer interwinding capacitance should have proper control or topological structure to handle the resulting high leakage inductance.

For the NSE:

1. A nonlinear source usually contains parasitic elements, such as a source capacitance in a PV system, which determines its dynamic behaviors. With the presence of the source capacitance, a PV system will take approximately hundreds of nanoseconds to tens of microseconds to finish a load transient. This quantity should be taken into account for the design of an NSE.

2. A nonlinear source output usually does not contain ripple. Therefore, it is desired that the NSE output ripple is as low as possible. This can be achieved by high-order filtering and stabilizing the switching frequency of the NSE.

3. An output voltage-controlled NSE may exhibit compromised controllability when operating close to the short circuit region of the I-V curve. Special attention should be paid to the controller design in order to maintain good performance along the whole I-V curve. Another possible solution is to use a dual-mode power circuit which consists of a voltage source and a current source, where the current source will take action when the NSE is within the short circuit region.

5.2 Future work

There are several possible challenges that have not been addressed in this work, and therefore could be subjects of future work. They are:

1. To solve the stability issue when the NSE operates in the short circuit region. One approach is to design a more robust control structure. Another approach is to use a dual-mode power circuit which consists of a separate voltage source and a separate current source power circuit. Deactivating the voltage source and activating the current source power circuit when the NSE operates in the short circuit region may solve the problem.

2. To solve the load step between nominal and short circuit. Once the stability issue in the short circuit region is solved, this issue may get easier to be solved.

3. To stabilize the switching frequency of the NSE by applying the method proposed in paper A.6. and verify the low output voltage ripple at all operating points.

4. To verify the common mode rejection of the proposed NSE system.

5. To investigate the current-controlled approach in order to verify its merits and limitations. A future work can implement and realize the proposed current controlled NSE in Fig. 4.24 into physical prototype.

Bibliography

[1] J.-G. Lim, S.-H. Kim, E.-K. Seo, H.-B. Shin, S.-K. Chung, and H. woo Lee, "Implementation of fuel cell dynamic simulator," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1–5, June 2006.

[2] J.-G. Lim and S.-K. Chung, "Implementation of a fuel cell dynamic simulator," *Journal of Power Electronics*, vol. 7, no. 4, pp. 336–342, 2007.

[3] C. Park, J. Liu, and P. Chou, "B#: a battery emulator and power-profiling instrument," *Design Test of Computers, IEEE*, vol. 22, pp. 150–159, March 2005.

[4] S. Poulsen, "Global loop integrating modulator," Nov. 23 2006. US Patent App. 10/556,210.

[5] S. Poulsen and M. Andersen, "Hysteresis controller with constant switching frequency," *Consumer Electronics, IEEE Transactions on*, vol. 51, pp. 688–693, May 2005.

[6] G. J. Madden and A. Le, "Solar panel model for design and analysis of power regulation equipment," *Proceedings of the Intersociety Energy Conversion Engineering Conference*, vol. 1, pp. 151–156, 1994.

[7] D. Schofield, M. Foster, and D. Stone, "Low-cost solar emulator for evaluation of maximum power point tracking methods," *Electronics Letters*, vol. 47, pp. 208–209, February 2011.

[8] S. Armstrong, C. K. Lee, and W. Hurley, "Investigation of the harmonic response of a photovoltaic system with a solar emulator," in *Power Electronics and Applications, 2005 European Conference on*, pp. 8 pp.–P.8, 2005.

[9] W. Kui, L. Yongdong, R. Jianye, and S. Min, "Design and implementation of a solar array simulator," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on*, pp. 2633–2636, Oct 2008.

[10] M. Cernaianu, C. Cirstea, and A. Gontean, "Cuk converter employing indirect current control loop for teg energy harvesting devices," in *Design and Technology in Electronic Packaging (SIITME), 2012 IEEE 18th International Symposium for*, pp. 193–196, Oct 2012.

[11] H. Nagayoshi, T. Nakabayashi, H. Maiwa, and T. Kajikawa, "Development of 100-w high-efficiency mppt power conditioner and evaluation of teg system with battery load," *Journal of electronic materials*, vol. 40, no. 5, pp. 657–661, 2011.

[12] T. Mesbahi, N. Rizoug, P. Bartholomeus, and P. Le Moigne, "Li-ion battery emulator for electric vehicle applications," in *Vehicle Power and Propulsion Conference (VPPC), 2013 IEEE*, pp. 1–8, Oct 2013.

[13] P. Chou, C. Park, J. Park, K. Pham, and J. Liu, "B#: a battery emulator and power profiling instrument," in *Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on*, pp. 288–293, Aug 2003.

[14] J. Ibirriaga, X. de Mendiluce Pena, A. Opritescu, D. Sera, and R. Teodorescu, "Low-cost, high flexibility i-v curve tracer for photovoltaic modules," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on*, pp. 1210–1215, May 2010.

[15] D. S. H. Chan and J. C. H. Phang, "Analytical methods for the extraction of solar-cell single- and double-diode model parameters from i-v characteristics," *IEEE Transactions on Electron Devices*, vol. 34, pp. 286–293, Feb 1987.

[16] S. K. Datta, K. Mukhopadhyay, S. Bandopadhyay, and H. Saha, "An improved technique for the determination of solar cell parameters," *Solid-State Electronics*, vol. 35, no. 11, pp. 1667 – 1673, 1992.

[17] S. Dib, M. De La Bardonnie, A. Khoury, F. Pelanchon, and P. Mialhe, "A new method for the extraction of diode parameters using a single exponential model," *Active and passive electronic components*, vol. 22, no. 3, pp. 157–163, 2000.

[18] D. Sera, R. Teodorescu, and P. Rodriguez, "Partial shadowing detection based on equivalent thermal voltage monitoring for pv module diagnostics," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pp. 708–713, Nov 2009.

[19] P. Acharya, P. Enjeti, and I. Pitel, "An advanced fuel cell simulator," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 3, pp. 1554–1558 Vol.3, 2004.

[20] J. Correa, F. Farret, J. Gomes, and M. Simoes, "Simulation of fuel-cell stacks using a computer-controlled power rectifier with the purposes of actual high-power injection applications," *Industry Applications, IEEE Transactions on*, vol. 39, pp. 1136–1142, July 2003.

[21] M. Ordonez, M. Iqbal, and J. Quaicoe, "Development of a fuel cell simulator based on an experimentally derived model," in *Electrical and Computer Engineering, 2005. Canadian Conference on*, pp. 1449–1452, May 2005.

[22] A. Thanheiser, T. Kohler, C. Bertram, and H. Herzog, "Battery emulation considering thermal behavior," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, pp. 1–5, Sept 2011.

[23] O. Konig, S. Jakubek, and G. Prochart, "Model predictive control of a battery emulator for testing of hybrid and electric powertrains," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, pp. 1–6, Sept 2011.

[24] O. Konig, C. Hametner, G. Prochart, and S. Jakubek, "Battery emulation for power-hil using local model networks and robust impedance control," *Industrial Electronics, IEEE Transactions on*, vol. 61, pp. 943–955, Feb 2014.

[25] "Two bipolar transistors form a low-cost solar-array emulator," December 2013.

[26] H. Nagayoshi, "Characterization of the module/array simulator using i-v magnifier circuit of a pn photo-sensor," in *Photovoltaic Energy Conversion, 2003. Proceedings of 3rd World Conference on*, vol. 2, pp. 2023–2026 Vol.2, May 2003.

[27] H. Nagayoshi, "*i-v* curve simulation by multi-module simulator using *i-v* magnifier circuit," *Solar Energy Materials and Solar Cells*, vol. 82, 2004.

[28] H. Nagayoshi and M. Atesh, "Partial shading effect emulation using multi small scale module simulator units," in *Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE*, pp. 1710–1713, Jan 2005.

[29] C.-H. Chang, E.-C. Chang, and H.-L. Cheng, "A high-efficiency solar array simulator implemented by an llc resonant dc-dc converter," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 3039–3046, June 2013.

[30] C. Chang, C. Cheng, and H. Cheng, "Modeling and design of the llc resonant converter used as a solar-array simulator," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, pp. 833–841, Dec 2014.

[31] S. Gadelovits, M. Sitbon, and A. Kuperman, "Rapid prototyping of a low-cost solar array simulator using an off-the-shelf dc power supply," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 5278–5284, Oct 2014.

[32] A. Koran, K. Sano, R. young Kim, and J.-S. Lai, "Design of a photovoltaic simulator with a novel reference signal generator and two-stage lc output filter," *Power Electronics, IEEE Transactions on*, vol. 25, pp. 1331–1338, May 2010.

[33] A. Koran, T. LaBella, and J.-S. Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 1285–1297, March 2014.

[34] Y. Kim, W. Lee, M. Pedram, and N. Chang, "Dual-mode power regulator for photovoltaic module emulation," *Applied Energy*, vol. 101, no. 0, pp. 730 – 739, 2013. Sustainable Development of Energy, Water and Environment Systems.

[35] O. Konig, S. Jakubek, and G. Prochart, "Battery impedance emulation for hybrid and electric powertrain testing," in *Vehicle Power and Propulsion Conference (VPPC), 2012 IEEE*, pp. 627–632, Oct 2012.

[36] R. Kumar, M. Suresh, and J. Nagaraju, "Effect of solar array capacitance on the performance of switching shunt voltage regulator," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 543–548, March 2006.

[37] M. A. E. Andersen, "Mos gate driver circuit with extremely high galvanic isolation," in *European Conference on Power Eletronics and Applications, EPE*, pp. 747–551, 1995.

[38] "Auxilliary power supplies for medium and high voltage applications," in *Bodo's Power System*, March 2011.

[39] S. Wang, P. Kong, and F. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1410–1416, 2007.

[40] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 6, pp. 1095–1099, 2003.

[41] D. Knurek, "Reducing emi in switch mode power supplies," in *Telecommunications Energy Conference, 1988. INTELEC '88., 10th International*, pp. 411–420, 1988.

[42] M. Borage, S. Tiwari, and S. Kotaiah, "Common-mode noise source and its passive cancellation in full-bridge resonant converter," in *Electromagnetic Interference and Compatibility, 2003. INCEMIC 2003. 8th International Conference on*, pp. 9–14, 2003.

[43] P. Kong, S. Wang, F. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1522–1533, 2011.

[44] W. Hong and R. O'Connell, "Effects of parasitic transformer capacitances on switching transients at a hv capacitor bank," in *Power Symposium, 2008. NAPS '08. 40th North American*, pp. 1–6, 2008.

[45] D. Garabandic, W. Dunford, and M. Edmunds, "Zero-voltage-zero-current switching in high-output-voltage full-bridge pwm converters using the interwinding capacitance," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 343–349, 1999.

[46] P. Kong and F. Lee, "Transformer structure and its effects on common mode emi noise in isolated power converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 1424–1429, 2010.

[47] "An-1095 design of isolated converters using simple switchers," April 2013. Application Note.

[48] "Miniature surface mount transformer," October 2013. Document 606-1.

[49] "Max250/max251 compatible converter transformers," – 2014. 78250 Series.

[50] A. J. Binnie and T. R. Foord, "Leakage inductance and interwinding capacitance in toroidal ratio transformers," *IEEE Transactions on Instrumentation and Measurement*, vol. 16, no. 4, pp. 307–314, 1967.

[51] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge llc resonant converter adopting boost pwm control scheme for hold-up state operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, pp. 841–850, Feb 2014.

[52] W. Feng, F. Lee, and P. Mattavelli, "Optimal trajectory control of llc resonant converters for led pwm dimming," *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, pp. 979–987, Feb 2014.

[53] W. Feng and F. Lee, "Optimal trajectory control of llc resonant converters for soft start-up," *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, pp. 1461–1468, March 2014.

[54] J. Biela and J. Kolar, "Using transformer parasitics for resonant converters - a review of the calculation of the stray capacitance of transformers," *IEEE Transactions on Industrial Applications*, vol. 44, no. 1, pp. 223–233, 2008.

[55] L. Dalessandro, F. da Silveira Cavalcante, and J. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081–2092, 2007.

[56] H.-Y. Lu, J. G. Zhu, and S. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1105–1112, 2003.

[57] Z. Ouyang, O. Thomsen, and M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power dc-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800–2810, 2012.

[58] T. Duerbaum and G. Sauerlaender, "Energy based capacitance model for magnetic devices," in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, vol. 1, pp. 109–115 vol.1, 2001.

[59] K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, "Minimization of the transformer interwinding parasitic capacitance for modular stacking power supply applications," in *The 16th European conference on Power Electronics and Applications, EPE'14 ECCE Europe*, 26–28 August 2014.

[60] K. Nguyen-Duy, Z. Ouyang, L. Petersen, A. Knott, O. Thomsen, and M. A. E. Andersen, "Design of a 300-w isolated power supply for ultra-fast tracking converters," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2014.

[61] K. Nguyen-Duy, L. Petersen, A. Knott, O. Thomsen, and M. A. E. Andersen, "Design of a 300-watt isolated power supply with minimized circuit input-to-output parasitic capacitance," in *The 7th IET international conference on Power Electronics, Machines and Drive, PEMD 2014*, 8–10 April 2014.

[62] K. Nguyen-Duy, A. Knott, and M. Andersen, "Loss performance analysis of an isolated power supply for ultrafast tracking converters," in *IEEE International Power Electronics and Application Conference and Exposition (IEEE PEAC'2014)*, pp. 1543–1548, November 2014.

[63] M. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Transactions on Power Electronics*, vol. 23, pp. 2387–2398, Sept 2008.

[64] M. Hoyerby and M. Andersen, "Carrier distortion in hysteretic self-oscillating class-d audio power amplifiers: Analysis and optimization," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 714–729, March 2009.

[65] K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "High dynamic performance solar array simulator oriented to ground testing of space applications," *to be submitted to IEEE Transactions on Power Electronics*, 2014.

[66] M. C. W. Høyerby and M. A. E. Andersen, "A small-signal model of the hysteretic comparator in linear-carrier self-oscillating switch-mode controllers," in *Nordic Workshop on Power and Industrial Electronics*, 2006.

[67] M. Hoyerby and M. A. E. Andersen, "Optimized envelope tracking power supply for tetra2 base station rf power amplifier," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, pp. 777–783, Feb 2008.

[68] "Mpp solar tracker: the effect of module temperature and insolation," November 2014.

[69] E. Koutroulis, K. Kalaitzakis, and V. Tzitzilonis, "Development of an fpga-based system for real-time simulation of photovoltaic modules," in *Rapid System Prototyping, 2006. Seventeenth IEEE International Workshop on*, pp. 200–208, June 2006.

[70] Y. Li, T. Lee, F. Peng, and D. Liu, "A hybrid control strategy for photovoltaic simulator," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 899–903, Feb 2009.

[71] C. Hametner, J. Unger, and S. Jakubek, "Local model network based dynamic battery cell model identification," in *Proceedings of the 11th WSEAS international conference on instrumentation, measurement, circuits and systems*, pp. 116–123, 2012.

[72] G. Gregorcic and G. Lightbody, "Local model network identification with gaussian processes," *Neural Networks, IEEE Transactions on*, vol. 18, pp. 1404–1423, Sept 2007.

[73] "Interlink coupling high-voltage impact isolation transformer," May 12 1999. CN Patent 2,318,700.

[74] "Medium-voltage high-speed switches with igbt power semiconductors," in *Bodo's Power System*, 04 December 2012.

[75] "Power electronics for medium-voltage applications," in *Bodo's Power System*, 25 February 2013.

[76] J.-h. Choi, M. Madafshar, and K. Parmenter, "Designing common-mode (cm) emi noise cancellation without y-capacitor," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, pp. 936–940, 2007.

[77] W. Xin, F. N. K. Poon, C. M. Lee, M. Pong, and Z. Qian, "A study of common mode noise in switching power supply from a current balancing viewpoint," in *Power Electronics and Drive Systems, 1999. PEDS '99. Proceedings of the IEEE 1999 International Conference on*, vol. 2, pp. 621–625 vol.2, 1999.

[78] D. Garabandic, W. Dunford, and M. Edmunds, "Snubbers for the distributed interwinding capacitance in high-output-voltage converters," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual*, vol. 2, pp. 846–849 vol.2, 1998.

[79] J. Sabate, V. Vlatkovic, R. Ridley, F. Lee, and B. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched pwm converter," in *Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual*, pp. 275–284, 1990.

[80] A. J. Binnie and T. R. Foord, "Leakage inductance and interwinding capacitance in toroidal ratio transformers," *IEEE Transactions on Instrumentation and Measurement*, vol. 16, no. 4, pp. 307–314, 1967.

[81] L. Mweene, C. Wright, and M. Schlecht, "A 1 kw 500 khz front-end converter for a distributed power supply system," *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 398–407, 1991.

[82] J. Sabate, V. Vlatkovic, R. Ridley, and F. Lee, "High-voltage, high-power, zvs, full-bridge pwm converter employing an active snubber," in *Applied Power Electronics Conference and Exposition, 1991. APEC '91. Conference Proceedings, 1991., Sixth Annual*, pp. 158–163, 1991.

[83] F. de Leon, S. Purushothaman, and L. Qaseer, "Leakage inductance design of toroidal transformers by sector winding," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 473–480, 2014.

[84] F. Blache, J.-P. Keradec, and B. Cogitore, "Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering," in *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE*, pp. 1211–1217 vol.2, 1994.

[85] D. Fu, S. Wang, P. Kong, F. Lee, and D. Huang, "Novel techniques to suppress the common-mode emi noise caused by transformer parasitic capacitances in dc-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4968–4977, 2013.

[86] L. Heinemann, J. Mast, G. Scheible, T. Heinzel, and T. Zuellig, "Power supply for very high insulation requirements in igbt gate-drives," in *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, vol. 2, pp. 1562–1566 vol.2, Oct 1998.

[87] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, pp. 3931–3940, Aug 2013.

[88] H. van Hoek, M. Neubert, and R. De Doncker, "Enhanced modulation strategy for a three-phase dual active bridge–boosting efficiency of an electric vehicle converter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, pp. 5499–5507, Dec 2013.

[89] G. Oggier, M. Ordonez, J. Galvez, and F. Luchino, "Fast transient boundary control and steady-state operation of the dual active bridge converter using the natural switching surface," *IEEE Transactions on Power Electronics*, vol. 29, pp. 946–957, Feb 2014.

[90] H. Qin and J. Kimball, "Closed-loop control of dc–dc dual-active-bridge converters driving single-phase inverters," *IEEE Transactions on Power Electronics*, vol. 29, pp. 1006–1017, Feb 2014.

[91] J.-W. Shin and B.-H. Cho, "Digitally implemented average current-mode control in discontinuous conduction mode pfc rectifier," *IEEE Transactions on Power Electronics*, vol. 27, pp. 3363–3373, July 2012.

[92] Y. Yan, F. Lee, and P. Mattavelli, "Analysis and design of average current mode control using a describing-function-based equivalent circuit model," *IEEE Transactions on Power Electronics*, vol. 28, pp. 4732–4741, Oct 2013.

[93] J. Wang and J. Xu, "Peak current mode bifrequency control technique for switching dc–dc converters in dcm with fast transient response and low emi," *IEEE Transactions on Power Electronics*, vol. 27, pp. 1876–1884, April 2012.

[94] M. Hallworth and S. Shirsavar, "Microcontroller-based peak current mode control using digital slope compensation," *IEEE Transactions on Power Electronics*, vol. 27, pp. 3340–3351, July 2012.

[95] Q. Zhang, C. Hu, L. Chen, A. Amirahmadi, N. Kutkut, Z. Shen, and I. Batarseh, "A center point iteration mppt method with application on the frequency-modulated llc microinverter," *IEEE Transactions on Power Electronics*, vol. 29, pp. 1262–1274, March 2014.

[96] M. Hoyerby and M. A. E. Andersen, "Teds base-station power amplifier using low-noise envelope tracking power supply," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 1687–1693, July 2009.

[97] Z. Housheng and Z. Yanlei, "Research on a novel digital photovoltaic array simulator," in *Intelligent Computation Technology and Automation (ICICTA), 2010 International Conference on*, vol. 2, pp. 1077–1080, May 2010.

[98] "Shunt-mode solar/wind charge controller," February 2014.

[99] "Series resisrance," November 2014.

[100] R. Kumar, M. Suresh, and J. Nagaraju, "Measurement of ac parameters of gallium arsenide (gaas/ge) solar cell by impedance spectroscopy," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 2177–2179, Sep 2001.

[101] R. A. Kumar, M. Suresh, and J. Nagaraju, "Measurement and comparison of {AC} parameters of silicon (bsr and bsfr) and gallium arsenide (gaas/ge) solar cells used in space applications," *Solar Energy Materials and Solar Cells*, vol. 60, no. 2, pp. 155 – 166, 2000.

[102] A. Patil, B. Cho, and F. Lee, "Design considerations for a solar array switching unit," in *Energy Conversion Engineering Conference, 1990. IECEC-90. Proceedings of the 25th Intersociety*, vol. 1, pp. 373–379, Aug 1990.

[103] B. Cho and D. Lee, *A single PWM section solar array shunt switching unit with an active ripple filter*. Dec 1995.

[104] J. M. Blanes, A. Garrigos, E. Sanchis-Kilders, and J. A. Carrasco, "A new sequential switching shunt regulator - digital shunt regulator (s3r-dsr) for solar array regulators," *IEEE International Symposium on Industrial Electronics*, vol. 2, pp. 1064–1069, 2006.

[105] A. Garrigos, J. Blanes, J. Carrasco, and J. Ejea, "Influence of the parasitic solar array capacitance in the sequential switching shunt series regulator," in *Electrotechnical Conference, 2006. MELECON 2006. IEEE Mediterranean*, pp. 1198–1201, May 2006.

[106] K. E. Shum and C. R. Ashley, "A new full shunt switching unit for solar array using coupled-inductor boost converter," *Proceedings of the Intersociety Energy Conversion Engineering Conference*, vol. 1, pp. 617–622 vol.1, 1996.

[107] K.-D. Rasch and K. Roy, "Shunt and blocking diodes for protection of space solar arrays.," *Conference Record of the IEEE Photovoltaic Specialists Conference*, pp. 550–553, 1981.

[108] C. K. Gowrishankara, K. P. Abhishek, and V. Krishnan, "Advanced solar array simulator," *Journal of Spacecraft Technology*, vol. 21, no. 2, pp. 13–23, 2011.

[109] J. M. Blanes, A. Garrigos, E. Sanchis, and J. A. Carrasco, "Modeling the sequential switching shunt series regulator," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 7–13, 2005.

[110] C. K. Gowrishankara and P. Pramada, "Switched mode power supply based solar array unit," *Proceedings of IEEE International Conference on Circuit, Power and Computing Technologies, ICCPCT 2013*, pp. 600–604, 2013.

[111] N. N. Goryashin and A. S. Sidorov, "Solar array regulator based on buck converter with sequential switched sections," *International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices, EDM*, pp. 364–368, 2013.

[112] K. Wu, "Loop gain of a spacecraft switched shunt power system," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 30, no. 4, pp. 1049–1053, 1994.

[113] M. Mira, A. Knott, O. Thomsen, and M. Andersen, "Boost converter with combined control loop for a stand-alone photovoltaic battery charge system," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, pp. 1–8, June 2013.

[114] K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "A review on the implementation of nonlinear source emulators," in *55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University*, pp. 56–62, October 2014.

[115] K. Nguyen-Duy, A. Knott, and M. Andersen, "Constant switching frequency self-oscillating controlled class-d amplifiers," *Elektronika ir Elektrotechnika*, vol. 20, no. 6, pp. 84–88, 2014.

List of publications

This section lists the publications accomplished during the PhD program. The detail manuscripts of each article are located in Appendix A.1.-A.7.

A.1.

K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "A Review on the Implementation of Nonlinear Source Emulators," in Proc. The 2014 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University, Riga, Latvia, 14 October 2014.

A.2.

K. Nguyen-Duy, L. P. Petersen, A. Knott, O. C. Thomsen, and M. A. E. Andersen, "Design of a 300-Watt Isolated Power Supply with Minimized Circuit Input-to-Output Parasitic Capacitance," in Proc. The 7th international conference on Power Electronics, Machines and Drives, Manchester, United Kingdom, 8-10 April 2014.

A.3.

K. Nguyen-Duy, Z. Ouyang, L. P. Petersen, A. Knott, O. C. Thomsen, and M. A. E. Andersen, "Design of a 300-W Isolated Power Supply for Ultrafast Tracking Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3319-3333, June 2015.

A.4.

K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, "Minimization of the Transformer Inter-winding Parasitic Capacitance for Modular Stacking Power Supply Applications," in Proc. The 16th European Conf. Power Elec. Appl., EPE'14 ECCE Europe, Finland, 26-28 August 2014.

A.5.

K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "Loss Performance Analysis of an Isolated Power Supply for Ultrafast Tracking Converters," in Proc. The IEEE International Power Electronics and Applications Conference and Exposition, Shanghai, China, 5-8 November 2014.

A.6.

K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "Constant Switching Frequency Self-Oscillating Controlled Class-D Amplifiers," Elektronika ir Elektrotechnika, vol. 20, no. 6, pp. 84-88.

A.7.

K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "High Dynamic Performance Nonlinear Source Emulator," *IEEE Transactions on Power Electronics*, accepted for publication on May 8, 2015.

Appendix A

Publications

This appendix contains the publications resulting from the Ph.D. program. Paper A.1. to A.6. have been presented or published in peer-reviewed conferences or transactions. Paper A.7. has been submitted for possible publication with the IEEE Transactions on Power Electronics.

A.1 (RTUCON2014)-A Review on the Implementation of Nonlinear Source Emulators

Paper A.1. is entitled "A Review on the Implementation of Nonlinear Source Emulators." Presented in The 2014 55th International Conference and Power and Electrical Engineering of Riga Technical University (RTUCON2014), Riga, LATVIA, 14 October, 2014.

A Review on the Implementation of Nonlinear Source Emulators

Khiem Nguyen-Duy (*Doctoral Student, Technical University of Denmark*),
Arnold Knott (*Associate Professor, Technical University of Denmark*)
and Michael A. E. Andersen (*Professor, Technical University of Denmark*)

***Abstract* – Renewable energy sources are playing an important role in industry as green sources of energy to reduce carbon dioxide emissions. They possess electrically nonlinear voltage-current characteristics. In the test and development of the downstream converters that utilize these renewable types of energy, the practice of using nonlinear source emulators instead of the real nonlinear sources has gained a lot of interest. Different methods of implementing nonlinear source emulators have been reported in the literature, but no paper exists reviewing and assessing them from different technical points of view. This paper provides a review of the implementation of existing nonlinear source emulators. Their configurations are redrawn as block diagrams and their circuit operations are discussed. Different industrial emulators are also briefly reviewed concerning their features.**

***Keywords* – Batteries, fuel cells, Photovoltaic systems, Renewable energy sources.**

I. Introduction

In the test and development of renewable energy based converters, the use of nonlinear source emulators (NSE) provides several advantages over the use of real non-linear sources. First, it requires a reduced test space compared to the use of usually large non-linear sources such as solar panels. Second, the cost of a test system with NSEs is usually less than that of a system with actual nonlinear sources [1]. One of the examples is that non-rechargeable batteries if were used in a test would have to be disposed after each test; hence, the test would be expensive and not friendly to the environment, but a battery emulator based on a power electronics system could be reused for a long time. Finally, an NSE provides flexible and reproducible test conditions for downstream converters because test conditions can be programmed or set inside the NSE [2], [3]. As a result, research on the development of NSE systems has been advanced recently.

Examples of the nonlinear source are the fuel cell, battery, thermoelectric generator [4], [5], and photovoltaic systems.

Considering a fuel cell system as a nonlinear source, the static V-I curve of a fuel cell emulator can be represented by a third-order polynomial as [6], [7]:

$$V = f(I) = \alpha_3 I^3 + \alpha_2 I^2 + \alpha_1 I + \alpha_0, \quad (1)$$

where V is the fuel cell terminal voltage, I is the fuel cell output current, and α_0 to α_3 are the coefficients of the static V-I curve and they change according to the changes of hydrogen concentration. Fig. 1 shows an example of the V-I curve characteristics of a fuel-cell system at different hydrogen concentration.

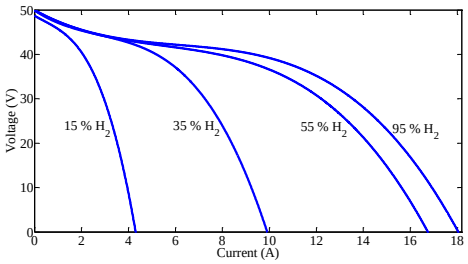


Fig. 1. Change of operating point due to changes of hydrogen concentration [6], [7].

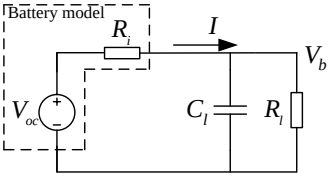


Fig. 2. A circuit model of a battery with load [8],[9].

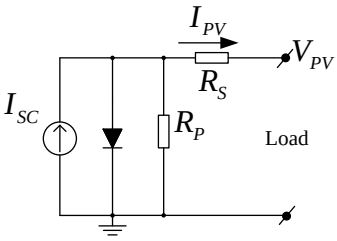


Fig. 3. The five-parameter model of a photovoltaic cell.

Batteries are also used extensively in industry such as in electric vehicle (EVs) or hybrid electric vehicle (HEVs) applications [8]–[10]. A circuit model of a battery connected with a load is shown in Fig. 2. It is noted that the model is usually utilized in the linear part of the V-I curve. The dashed area models a battery, in which, V_{oc} and R_i are the open-circuit voltage and internal resistance, respectively. The rest of the circuit models a load with a capacitance C_l and resistance R_l. The load is not necessarily fixed; it can vary in time with activities and power management policies [8], [10]. The available voltage at the output of the battery is:

$$V_b = V_{oc} - IR_i. \quad (2)$$

During the discharge of the battery, V_{oc} decreases while R_i increases; both of them are based on the state of the battery and its internal temperature.

In case of a photovoltaic system, the *five-parameter model* is widely used to describe the system's electrical characteristic.

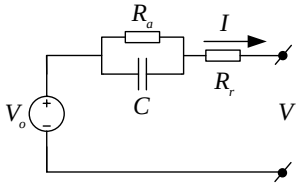


Fig. 4. An ac equivalent circuit model of fuel cell [6], [7].

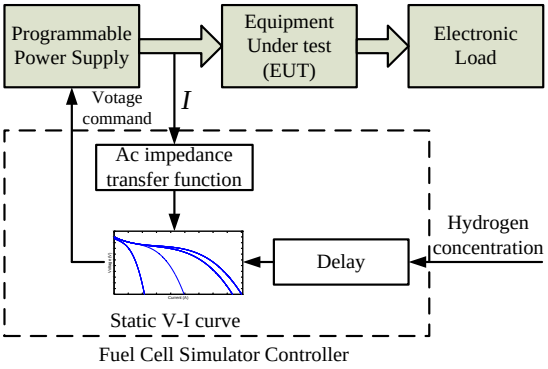


Fig. 5. Control block diagram of the fuel cell emulators proposed in [6], [7].

The model is shown in Fig. 3 [11], [12]. It is also called the *single diode detailed model*. The current is related to the terminal voltage V_{PV} and the short circuit current I_{SC} by:

$$I_{PV} = I_{SC} - I_o\left(e^{\frac{V_{PV}+I_{PV}R_S}{n_S V_t}} - 1\right) - \frac{V_{PV}+I_{PV}R_S}{R_P}, \qquad (3)$$

where R_P models the loss due to leakage currents across the junction, R_S models the internal series resistance, I_o is the dark saturation of the diode, V_t is the module thermal voltage, and n_s is the number of series connected cells in the module. The short circuit current I_{SC} is affected by the solar irradiance and the open circuit voltage V_{OC} is affected by the cell temperature. Normally, R_P is relatively large and R_S is relatively small. In practice, the model can be reduced further to the *four-parameter model* where the shunt resistor R_P is neglected. In some cases, the series resistor R_S is also neglected, resulting in a much simplified model, where:

$$I_{PV} = I_{SC} - I_o\left(e^{\frac{V_{PV}}{n_S V_t}} - 1\right). \qquad (4)$$

This paper focuses on the review of the technical implementation of existing NSEs in the literature. The background of each NSE and the concept of each implementation are reviewed and discussed. It is noted that different industrial products such as [27]-[29] exist for such function as NSEs, but their implementation is not available. Therefore, several industrial products are only briefly reviewed here in terms of their features. Comparisons are being made among the non-commercial emulators only.

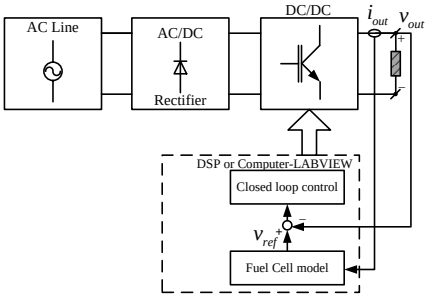


Fig. 6. Control block diagram of the fuel cell emulators proposed in [14] and [15].

II. Fuel Cell Emulators

A. Review of existing works

In this section, the fuel cell simulator is reviewed. An ac equivalent circuit model is shown in Fig. 4 which is used to simulate the dynamic characteristics for load changes at a given dc operating point. According to [6], [7] and from Fig. 4, the ac output impedance of a fuel cell can be modelled as:

$$\frac{V(s)}{I(s)} = K_{stat}\left(\frac{R_r}{R_a+R_r}.\frac{s+(R_a+R_r)/(R_aR_rC)}{s+(1/R_aC)}\right). \qquad (5)$$

where $K_{stat} = R_a + R_r$ models the impedance at the dc operating point which can be obtained from the static V-I curve.

References [6], [7] introduce a fuel cell emulator implemented by using a programmable dc power supply and LabVIEW graphical user interface. To simulate the changes of load, a programmable electronic load is used. The system emulates the electrical behaviors of an actual proton exchange membrane fuel cell (PEMFC). The block diagram of the control system is shown in Fig. 5. The operation of the system is as follows.

The programmable dc power supply is connected to equipment under test (EUT) and an electronic load is connected to the EUT. The output current is sensed and passed through a programmed ac impedance transfer function shown in equation (5) in order to generate a dynamic change in output voltage reference. The hydrogen concentration is delayed and sent to the static V-I curve block that determines which static V-I curve the emulator is operating in. The command voltage is the reference for the programmable power supply to ge-nerate the require output voltage. Based on that control struc-ture, the whole system is able to simulate the dynamic change of static curve due to hydrogen change as well as the dynamic change of output voltage when the load current changes.

The work reported in [13] discusses a 5 kW solid oxide fuel cell (SOFC). It uses a cubic polynomial curve-fitting technique with the equation of the same form like (1) in order to interpolate the missing data between the data obtained from the experiments. The work also considers the system like having voltage source connected in series with a non-linear internal impedance. The dynamic change of load is assumed to make a slow change in output power of the SOFC and therefore, the works simulate the power change by adjusting the current limit on the power supply.

TABLE I.

SPECIFICATIONS AND CHARACTERISTICS OF EXISTING FUEL CELL EMULATORS

Reference	Power rating	Power stage	Simulated fuel cell	Dynamic load change simulation	H_2 concentration change simulation
[6], [7]	2 kW	Commercial PS	PEMFC	Yes	Yes
[13]	5 kW	Commercial PS	SOFC	Yes	Yes
[14]	Not found	Custom made	DMFC	Yes	No
[15]	500 W	Custom made	PEMFC	Yes	No

TABLE II.

SPECIFICATIONS AND CHARACTERISTICS OF EXISTING BATTERY EMULATORS

Reference	Power rating	Power stage	Simulated battery	Thermal model
[8], [9]	Not found	Adjustable linear regulator	Li-Ion	No
[10]	Not found	Bidirectional dc-dc converter	Li-Ion	No
[16]	Not found	Commercial PS	Li-Ion	Yes
[17], [18]	60 kW	Three-phase interleaved buck	Not found	No

The works introduced in [14], [15] have utilized a switch-mode power converter as the power circuit. The control block diagram proposed in [14], [15] is shown in Fig. 6. In [14], a synchronous buck converter is the main power converter and it is controlled by a low cost fixed point digital signal processor (DSP). The paper utilizes an empirical model of a direct methanol fuel cell (DMFC) instead of the electro-chemistry equation in order to reduce computational complexity. Although the paper was working on the DMFC, it claimed that the procedure to build an empirical model can be extended to other fuel cells. The output voltage and output current are read and fed back to a DSP. The DSP reads the feedback current and computes the reference voltage based on the fuel cell model. This reference is compared to the feedback voltage. The error is then used in a sliding mode controller to control the output of the buck converter. The simulation when the hydrogen concentration is changed is not reported. In [15], a PEMFC system is emulated. The approach is of the same kind with [14]. However, instead of using a DSP, [15] LabVIEW to perform all of the control is applied.

B. Evaluation

Table I summarizes the specifications and characteristics of the reviewed fuel cell emulators. Due to the complexity, most emulators have been developed with advanced digital control unit such as LabVIEW based FPGA or DSP. The availability of a GUI in [6], [7], [13], and [15] provide advantage in changing parameters as well as in extending the simulation to other types of fuel cells. Despite being low-cost, [14] is less flexible due to the limited computational capability of the low cost DSP and it may be suitable for laboratory testing only. It depends on the requirement on flexibility, development time and cost to select an implementation approach. If high flexibility and short development time is aimed, then a system consists of commercial power supply controlled by FPGA with GUI could be recommended, such as in [6], [7] and [13]. For low-cost oriented system, a system consists of a basic power converter prototype controlled by a low-cost DSP is recommended, such as in [14].

III. BATTERY EMULATORS

Batteries have been used in EVs or HEVs to reduce the pollution created by gasoline engines. Different battery technologies that can be used as a storage system exist. They are Nickel-Cadmium (Ni-Cd), Nickel-Metal Hydride (Ni-MH), and Lithium-Ion (Li-Ion) [10].

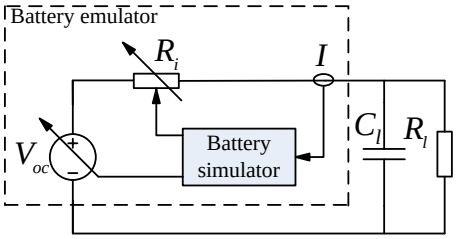


Fig. 7. A circuit model of a battery emulator with a load [8], [9].

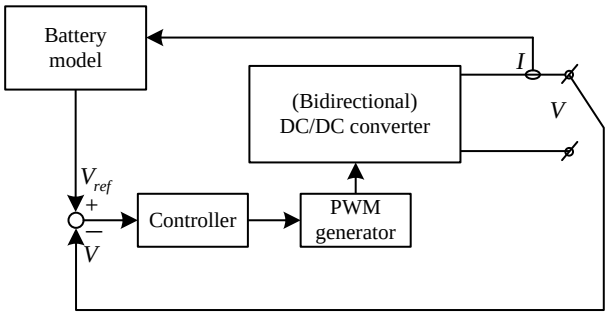


Fig. 8. An implementation of battery emulator with switching power supply as power stage [10].

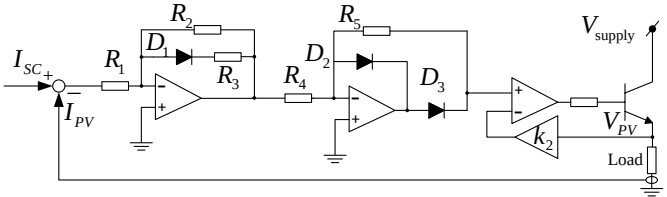


Fig. 9. PV emulator circuit 1 [1].

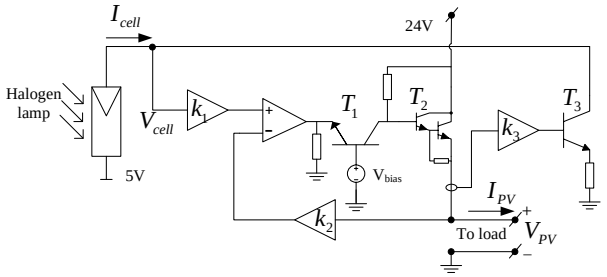


Fig. 10. PV emulator circuit 2 [2].

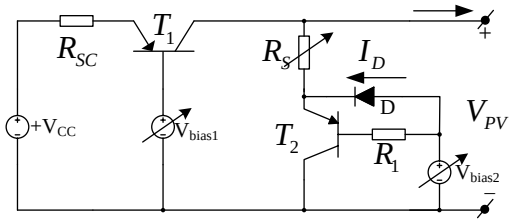


Fig. 11. PV emulator circuit 3 [22].

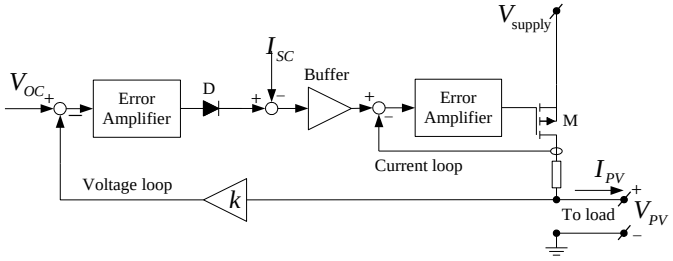


Fig. 12. PV emulator circuit 4 [3].

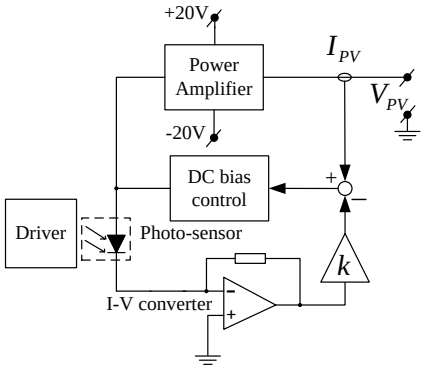


Fig. 13. PV emulator circuit 5 [30].

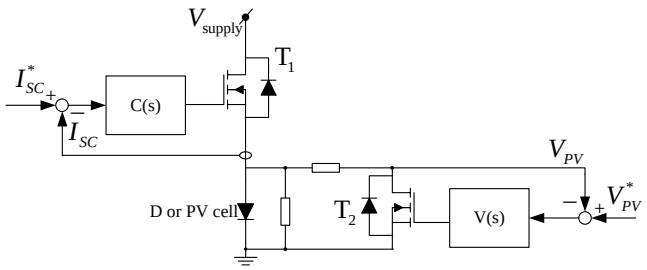


Fig. 14. PV emulator circuit 6 [23].

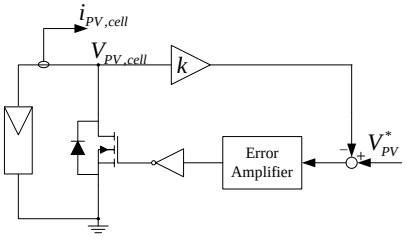


Fig. 15. PV emulator circuit 7 [24].

In [8], [9] a battery emulator is developed based on a programmable power supply controlled by a micro-controller and a host computer. The emulator is claimed to be able to collect power profiles through real-time measurements and save the data to a file in the emulator's profiling mode. It also has a training mode where actual battery can be connected for calibrating a simulation model.

The operation concept of the system in [8], [9] is as follows. The concept is shown in the circuit model in Fig. 7. Two variables, namely the current *I* and the temperature *T* are measured. After that, the battery simulator implemented inside a DSP processes the information and compute the set-point for the open circuit voltage V_{oc} and R_i. In implementation, an adjustable linear regulator is used to output the open circuit voltage. Because the internal resistance of the linear regulator used is already larger than the desired battery internal resistance R_i, there is no passive resistor added to the circuit. The battery internal resistor is implemented by adjusting the open circuit voltage command to compensate for the voltage drop across it. The control is performed by a micro-controller.

In [10], a Li-Ion battery emulator is also proposed. The concept of the circuit model can also be described in Fig. 8. Instead of using a linear voltage regulator such as that in [8] and [9], reference [10] uses a bidirectional dc/dc converter fed by a power supply. The control system is implemented by a dSPACE board controlled by a MATLAB/Simulink environment.

Reference [16] also utilizes a programmable power supply. The difference is that the control system is handled with a hardware in the loop (HiL) environment. As the thermal behavior strongly affects the parameters of a battery model, this behavior has been taken into account in [16]. Specifically, a thermal model has been proposed in the work.

References [17]–[19] propose the design of battery emulators for hybrid and electric powertrain testing. Specifically, [19] uses a local model network (LMN) [20], [21] that can be used to emulate any type of battery chemistry or any other electrical energy storage system.

It is also worth visiting the industrial battery emulators. References [27] and [28] discuss the commercial battery simulator and battery/charger simulators. They were targeted on test applications of portable, battery operated product such as cellular and cordless telephones, mobile radios, and pagers, which are all low power consumption devices. They can be used to simulate a discharged battery for charger testing. In portable power wireless devices, the load current transient from standby mode to full-power RF transmission can

perform a rapid change of as much as 1000 % instantaneously; for example, from 100-300 mA to 1-3 A. This makes the battery voltage to drop rapidly due to the presence of the internal resistance. As models [27] and [28] possess programmable internal resistances with a high resolution, they are suitable for testing of those portable wireless devices.

Table II summarizes the specifications and characteristic of the existing battery emulators in the literature. The industrial products [27], [28] are not included into the table because they are designed for different applications.

IV. Photovoltaic Emulators

A. Review of existing works

To simplify the schematics of the reviewed photovoltaic emulators, redrawn schematics are introduced, which treat current measurement by the current sensing symbol. The summation circuits are redrawn with summation signal symbols. The circuits that interface the power switches and the driving signals are redrawn as the driver.

The first circuit to review is reported in [1] and is re-drawn in Fig. 8. It is constructed based on the simplified single diode model with equation (4). Rearranging the equation, the terminal voltage can be derived as:

$$V_{PV} = V_T \ln\left(\frac{I_{SC} - I_{PV}}{I_0} + 1\right). \quad (6)$$

Referring to the schematic, the short circuit current I_{SC} is subtracted from the output emulator current I_{PV} and scaled by $1/I_0$. After that, the first operational amplifier (Op-amp) circuit takes the natural logarithmic function, but the result is opposite in polarity.

The second Op-amp in Fig. 9 is a precision rectifier that rectifies the signal to fulfil equation (6). Finally, a driver circuit and a power stage with transistor are used to provide voltage gain as well as current gain for the output. The circuit is to simulate a 12 W thin film silicon solar cell. The power rating is limited by the rated current flowing through the power transistor and the output voltage limited by V_{supply}.

Circuit 2 is shown in Fig. 10 [2]. It uses a small single photovoltaic cell the maximum power of which is 17 mW and a dc halogen lamp in order to create a photovoltaic effect. The dc halogen lamp, the brightness of which can be adjusted, illuminates the low power photovoltaic cell in order to model the suns irradiance of a photovoltaic system. The output current of the circuit is sensed by a series resistor and converted to a voltage that drives the base of the power transistor. In this way, the current draw from the photovoltaic cell and the output current are proportional. The photovoltaic cell voltage is amplified by the common base circuit. The system produces an output of 50 W. The power rating is limited by the rated current flowing through the Darlington transistor and the output voltage limited by the rail voltage of 24 V.

Circuit 3 is shown in Fig. 11 and introduced in [22]. The circuit allows adjustment of the three most important variables: V_{bias1} for the short circuit current I_{SC}, V_{bias2} for the voltage at maximum power point V_{MPP} , and R_S for the series resistor. The short circuit current I_{SC} is determined by V_{bias1} ; it passes through transistor T_1. Its value is $I_{SC} = (+V_{CC} - V_{bias1})/R_{SC}$. When the circuit operates near the short circuit region, the output voltage is small, and emitter voltage of T_2 is small; it is clamped by diode D and $V_{E2} = V_{bias2} - V_D$, where V_D is the forward voltage drop of D. When the load decreases, the output voltage increases. Diode D is reverse biased and T_2 starts to conduct. The output current is the subtraction of the short circuit current from the transistor current. The power rating is 12 W. The limitation in the power rating is due to similar reasons as those in circuit 1 and 2.

Circuit 4 was proposed in [3] and re-drawn in Fig. 12. There are two feedback loops used: a current feedback loop to set the short circuit current, and a voltage feedback loop that determines the open circuit voltage. When the feedback voltage of V_{PV} is smaller the reference voltage V_{OC} , the output of the error amplifier is negative and diode D is off. The output current is therefore regulated at the short circuit current by the current loop. When the load becomes lighter, or the output voltage increases, the output of the error amplifier is positive and diode D is forward biased. The new reference for the output current is the subtraction of the short circuit current from the diode current. The higher the output voltage, the higher the current flowing through the diode and the output current decreases according to the I-V curves toward the open circuit point. The output power was 61 W. The limitation in the power rating is due to similar reason as in circuit 1, 2 and 3.

Circuit 5 [30] is re-drawn by block diagram in Fig. 13. The power rating of this circuit is 30W. A photo sensor with output current of less than 100 μA is used to imitate the solar panel. The supply voltage of the power Op-amp is ±20V. The output of the photo-sensor is converted to voltage by a current-to-voltage converter with FET-input Op-amp in order to reduce the effect of bias current in Op-amps with bipolar-junction-transistor inputs. The current gain is adjusted by the gain of the I-V converter. The measured output current is compared with the photo-sensor current and processed by a DC bias controller. The output of the controller determines the operating point of the power circuit, and is amplified by the power amplifier circuit. The power rating is limited by the capability of the power Op-amp used.

Circuit 6 [23] is re-drawn by block diagram in Fig. 14. It uses the five-parameter model of a PV system. There are four diodes in series to model an actual PV cell characteristic, and later, a real PV cell is used. There are two control loops: the current loop C(s) regulates the short circuit current by controlling MOSFET T_1 in its linear region. In a similar concept, controller V(s) ensures that the output voltage tracks the output voltage reference by controlling MOSFET T_2 in its linear region. The current loop has a cross over frequency of 90 kHz and its phase margin is 60° while the voltage loop has a cross over frequency of 20 kHz and a phase margin of 50^0.

TABLE III.

SPECIFICATIONS AND CHARACTERISTICS OF EXISTING PHOTOVOLTAIC EMULATORS

Circuit	V_{OC} (V)	I_{SC} (A)	MPPT (W)	Partial shading simulation
1	22	0.31	4	No
2	21.57	3.44	50	Yes
3	20	0.9	12	No
4	70	1.16	61	No
5	16	2.5	30	Yes
6 (with power stage)	250	20	2700	Yes
7 (with power stage)	200	20	2000	Yes

The power rating with power stage is 2.7 kW and is mainly limited by the design of the buck-converter power stage.

Circuit 7 [24] is redrawn by a block diagram in Fig. 15. A PV cell is illuminated to generate the I-V curve characteristic. The voltage of the PV cell is controlled to track the reference voltage. The resulting current of the PV cell is used as the reference output current for the power stage which is based on a three-phase interleaved buck dc-dc converter whose output power is 2.0 kW.

The Chroma solar array simulator [29] contains basically all important features of a solar panel. It can also simulate partial shading effect and static and dynamic MPPT efficiency test. The users are also able to import real conditions of irradiation and temperature profiles of a whole day from an excel file to an associated software. The model series is able to connect multiple solar array simulators in parallel with automatic current sharing control when high power, for example, up to 1 MW, is required.

B. Evaluation

1) Partial shading simulation ability

In terms of simulation of advanced feature of the NSE such as the partial shading effect, the methods that use actual PV cells or photo censors such as circuit 2,5,6, and 7 possess an advantage over the use of diodes or transistors in the other circuits. The partial shading effect was neither investigated in circuit 2 nor circuit 6, but it might be implemented by adding bypass diode to the solar cell and covering part of the solar cell. In circuit 5 [5], the partial shading was implemented by a proper series connection of the I-V magnifier circuits. In circuit 7, the partial shading effect was produced by connecting two reference cells in series, each of them had one bypass diode, and one of the two cells was partially shaded. One observation is that, it might get much more complicated to simulate the partial shading effect with analog circuits in which diodes or junction of transistors are usually used to model the exponential curves.

2) Accuracy

As comparison to the real non-linear source characteristics were missing in all of the circuits being reviewed except for circuit 1, it is difficult to assess the accuracy of the reviewed photovoltaic emulators or to make a comparison among them. However, it has been seen that the series resistor and shunt resistor are usually neglected to simplify the circuit, such as in circuit 1, 2, and 3. Although being simplified, it is very interesting to see that the experiments in circuit 1 matched fairly well with the photovoltaic cell being simulated. This is reasonable because the shunt resistor is usually large and the series resistor is usually small; hence, in some particular cases they can be ignored. The claim accuracy is 5.4 % error in the actual maximum power level. Circuit 3 takes into account the series resistance but not the shunt resistance; it can be improved further by adding a shunt resistor into the circuit. Circuit 6 is the closest to the five-parameter model with both the shunt and series resistor presented and is expected to produce small signal I-V curves that match better with the real I-V curve. Table III summarizes the specifications and partial shading functions of the reviewed emulators.

One observation is that, the presence of a p-n junction from either diode(s) or the base-emitter of transistor(s) in order to produce the exponential function is vital to the implementation of the analogue photovoltaic emulators. It is also noted that, simulation of the I-V curve by digital control is also very popular, such as reported in [25], [26]. In this kind of methods, I-V curve data are stored in the memory of the digital unit, or the I-V curve is computed by mathematical equation and approximating method. A future study will cover the digital implementation of the photovoltaic emulators.

V. CONCLUDING REMARKS

The change of hydrogen concentration in a fuel cell system is analogous to the change of solar irradiation in a solar panel because they both cause a change in the short circuit current. However, there is a considerable delay from the change of the hydrogen concentration until the fuel cell reacts, whereas the change of solar irradiation has an almost instantaneous effect to the operating point of a solar panel. Therefore, simulation of a fuel cell system requires less control bandwidth than simulation of a PV system. The partial shading effect of a photovoltaic system also complicates the simulation of a PV system.

In general, most laboratory testing prototypes reported tend to try to resemble the most basic electrical characteristics of the non-linear source. They also tend to simplify or ignore the other characteristics such as the hydrogen concentration change in fuel cell emulators, the thermal behavior in battery emulators, and the partial shading effect in PV emulators.

In this paper, the authors have presented a literature review of different implementation methods of the NSEs. Their control block diagrams have been presented. Furthermore, system operations have been reviewed. The specifications and characteristics of existing methods have also been analyzed. In addition, the existing works have been compared side by side and several commercial devices of the same kind are briefly reviewed. In general, this paper has provided a broad picture of the existing NSEs. It can foster and inspire the implementation of them.

REFERENCES

[1] D. Schofield, M. Foster, and D. Stone, "Low-cost solar emulator for evaluation of maximum power point tracking methods," *Electronics Letters*, vol. 47, no. 3, pp. 208–209, February 2011.

[2] S. Armstrong, C. K. Lee, and W. Hurley, "Investigation of the harmonic response of a photovoltaic system with a solar emulator," in *Proc. 2005 Euro. Conf. Power Electron. Appl.*, 2005, pp. 8 pp.–P.8.

[3] W. kui, L. Yongdong, R. Jianye, and S. Min, "Design and implementation of a solar array simulator," in *Int. Conf. Electrical Mach. Sys., 2008*, Oct 2008, pp. 2633– 2636.

[4] M. Cernaianu, C. Cirstea, and A. Gontean, "Cuk converter employing indirect current control loop for teg energy harvesting devices," in *Proc. IEEE 18th Int. Sym. Design Tech. Electron. Pack. 2012*, Oct 2012, pp. 193–196.

[5] H. Nagayoshi, T. Nakabayashi, H. Maiwa, and T. Kajikawa, "Development of 100-w high-efficiency MPPT power conditioner and evaluation of TEG system with battery load," *Journal of electronic materials*, vol. 40, no. 5, pp. 657–661, 2011.

[6] [6] J.-G. Lim, S.-H. Kim, E.-K. Seo, H.-B. Shin, S.-K. Chung, and H. woo Lee, "Implementation of fuel cell dynamic simulator," in *37th IEEE Power Electron. Specialists Conf., 2006.*, June 2006, pp. 1–5.

[7] J.-G. Lim and S.-K. Chung, "Implementation of a fuel cell dynamic simulator," *Journal of Power Electron.*, vol. 7, no. 4, pp. 336–342, 2007

[8] C. Park, J. Liu, and P. Chou, "B#: a battery emulator and power-profiling instrument," *Design Test of Computers, IEEE*, vol. 22, no. 2, pp. 150–159, March 2005.

[9] P. Chou, C. Park, J. Park, K. Pham, and J. Liu, "B#: a battery emulator and power profiling instrument," in *Proc. 2003 Int. Sym. Low Power Electron. Design*, Aug 2003, pp. 288–293.

[10] T. Mesbahi, N. Rizoug, P. Bartholomeus, and P. Le Moigne, "Li-ion battery emulator for electric vehicle applications," in *Proc. 2013 IEEE Vehicle Power Propulsion Conf.*, Oct 2013, pp. 1–8.

[11] J. Ibirriaga, X. de Mendiluce Pena, A. Opritescu, D. Sera, and R. Teodorescu, "Low-cost, high flexibility i-v curve tracer for photovoltaic modules," in *12th Int. Conf.Optimization Electrl. Electron. Equipment 2010*, May 2010, pp. 1210–1215.

[12] D. S. H. Chan and J. C. H. Phang, "Analytical methods for the extraction of solar-cell single-and double-diode model parameters from I-V characteristics," *IEEE Trans. Electron Devices*, vol. 34, no. 2, pp. 286– 293, Feb 1987.

[13] P. Acharya, P. Enjeti, and I. Pitel, "An advanced fuel cell simulator," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 3, 2004, pp. 1554–1558 Vol.3.

[14] M. Ordonez, M. Iqbal, and J. Quaicoe, "Development of a fuel cell simulator based on an experimentally derived model," in *2005. Canadian Conf., Electrl Computer Eng.*, May 2005, pp. 1449–1452.

[15] J. Correa, F. Farret, J. Gomes, and M. Simoes, "Simulation of fuel-cell stacks using a computer-controlled power rectifier with the purposes of actual high-power injection applications," *Industry Applications, IEEE Transactions on*, vol. 39, no. 4, pp. 1136–1142, July 2003.

[16] A. Thanheiser, T. Kohler, C. Bertram, and H. Herzog, "Battery emulation considering thermal behavior," in *Vehicle Power and Propulsion Conf., 2011 IEEE*, Sept 2011, pp. 1–5.

[17] O. Konig, S. Jakubek, and G. Prochart, "Model predictive control of a battery emulator for testing of hybrid and electric powertrains," in *Vehicle Power and Propulsion Conference, 2011 IEEE*, Sept 2011, pp. 1– 6.

[18] O. Konig, S. Jakubek and G. Prochart,"Battery impedance emulation for hybrid and electric powertrain testing," in *Proc. 2012 IEEE Vehicle Power and Propulsion Conf.*, Oct 2012, pp. 627–632.

[19] O. Konig, C. Hametner, G. Prochart, and S. Jakubek, "Battery emulation for power-hil using local model networks and robust impedance control," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 943– 955, Feb 2014.

[20] C. Hametner, J. Unger, and S. Jakubek, "Local model network based dynamic battery cell model identification," in *Proc. the 11th WSEAS int. conf. instrumentation, measurement, cir . sys.*, 2012, pp. 116–123.

[21] G. Gregorcic and G. Lightbody, "Local model network identification with gaussian processes," *Neural Networks, IEEE Transactions on*, vol. 18, no. 5, pp. 1404–1423, Sept 2007.

[22] "Two bipolar transistors form a low-cost solar-array emulator," December 2013. [Online]. Available: http://electronicdesign.com/energy/two bipolar- transistors-form-low-cost-solar-array-emulator

[23] Koran, A.; Sano, K.; R.-Y Kim, and J.-S Lai, "Design of a photovoltaic simulator with a novel reference signal generator and two-stage LC output filter," *IEEE Trans. Power Electron.*, vol.25, no.5, pp.1331,1338, May 2010.

[24] Koran, A.; LaBella, T., and J.-S Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *IEEE Trans. Power Electron.*, vol.29, no.3, pp.1285,1297, March 2014.

[25] E. Koutroulis, K. Kalaitzakis, and V. Tzitzilonis, "Development of an fpga- based system for real-time simulation of photovoltaic modules," in *Proc. 17th IEEE Int. Workshop Rapid Sys. Prototyping*, June-2006, pp. 200–208.

[26] Y. Li, T. Lee, F. Peng, and D. Liu, "A hybrid control strategy for photovoltaic simulator," in *Proc. 24th Annual IEEE Appl. Power Electron. Conf. Expo.*, Feb 2009, pp. 899–903.

[27] (2014). Model 2302 DC Power Supply Single Channel Battery Simulator.[Online].Available: http://www.keithley.com/products/dcac/highspeedpower/battery/?mn=2302

[28] (2014). Model 2306 DC Power Supply, Dual-Channel Battery/ Charger Simulator.[Online]. Available: http://www.keithley.com/products/dcac/highspeedpower/battery/?mn=2306

[29] (2014). Model 62000H-S series Solar Array Simulator. [Online]. Available: http://www.chromaate.com/product/62150H- 600S_1000S_Solar_Array_Simulator.htm

[30] Hiroshi Nagayoshi, "I–V curve simulation by multi-module simulator using I–V magnifier circuit," Solar Energy Materials and Solar Cells, Volume 82, Issues 1–2, 1 May 2004, Pages 159-167, ISSN 0927-0248

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A.2 (PEMD2014)-Design of a 300-Watt Isolated Power Supply with Minimized Circuit Input-to-Output Parasitic Capacitance

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Design of a 300-Watt Isolated Power Supply with Minimized Circuit Input-to-Output Parasitic Capacitance

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Keywords: Current transformers, parasitic capacitance, switching converters, stacking, dc-dc power converters.

Abstract

This paper presents the design of a 300-Watt isolated power supply for MOS gate driver circuit in medium and high voltage applications. The key feature of the developed power supply is having a very low circuit input-to-output parasitic capacitance, thus maximizing its noise immunity. This makes it suitable for modular stacking applications. The converter is a voltage-controlled current source, utilizing a transformer that has an extremely low inter-winding parasitic capacitance. The experiments show that an overall circuit input-to-output parasitic capacitance of 10 pF can be achieved. Design analysis and experimental results are provided to prove the feasibility of the converter.

1 Introduction

Research on common-mode noise mitigation has received great attention since the introduction of electromagnetic interference (EMI) regulations [1-8]. Among the existing approaches, design of transformers with minimized inter-winding parasitic capacitance and utilization of suitable topologies is a very typical approach. In [1], an unusual transformer winding structure and an unconventional converter topology were proposed. The system achieved 1 pF parasitic capacitance at its output power of 36 V, 0.2 A. Later on, similar approaches [2]-[4] were proposed using a similar transformer structure. Nevertheless, the reported previous works provided neither experimental results nor elaborate analysis of the converter's operation.

This paper seeks to further investigate and validate the merit of the converter topology in Fig. 1 which was firstly proposed in [1]. A higher output power rating is aimed, which is 300 W per module. The prototype is built in a way that minimizes the circuit input-to-output parasitic capacitance, making it less susceptible to noise and suitable for modular stacking. The overall circuit input-to-output parasitic capacitance is 10-pF, which, to the authors' best knowledge, is the lowest of their kind with 300 W output power rating.

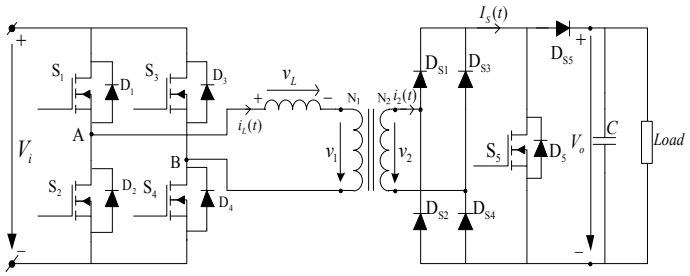


Fig. 1. Topology of the proposed converter.

2 System requirements

Referring to the converter in Fig. 1, the input dc supply voltage of the converter is usually the output of a power factor correction converter which converts a single phase 220-V ac voltage into 400 V dc voltage. Therefore, a dc input of 400 V is chosen in the design. The output voltage is chosen to be 60 V dc, since it allows a variety of power switch selections which have a breakdown voltage of 100 V dc. If, for example, higher output voltage is desired, then more than one converter modules can be stacked in series. The output current is designed to be 5 A maximum. This specification means the maximum output power that is available in the output terminals is 300 W. Furthermore, an extremely low total circuit input-to-output parasitic capacitance of 10 pF is aimed. All of these specifications are stated in Table 1.

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Circuit input-to-output capacitance	10 pF

Table 1. Design specification

3 Common mode noise paths

The common mode noise paths are shown in Fig. 2. In this topology, the nodes that have high dv/dt are nodes A, B, X, Y, and Z. In nodes A and B, there are changes of voltage from $\pm V_i$ to $\mp V_i$ with respect to the primary side return. Nodes X, Y, Z see a change of 0 V to 60 V with respect to the

secondary side return. These nodes are the sources of common mode noise currents. In the developed prototype, there are two heat-sinks used, one for each side to reduce the capacitive coupling between the two sides. Since the drains of switch S_2 and S_4 are switching nodes and they are both attached to heat-sink 1, the coupling paths include capacitances from drains of S_2 and S_4 to heat-sink 1, and capacitance from heat-sink 1 to chassis/earth. In implementation practice, the heat-sink can be electrically connected to the return path (not the chassis/earth) to further mitigate the transmission of common mode noise current. The coupling paths in the secondary side include the capacitances from cathode of $D_{S1}, D_{S2}, D_{S3}, D_{S4}$ and the drain of S_5 to heat-sink 2, and capacitance from heat-sink 2 to chassis/earth. The coupling path caused by the transformer is from the inter-winding capacitance C_{int}. It can be clearly seen that, C_{int} is in series with the other coupling capacitances, forming a loop of common mode noise paths. Therefore, the value of C_{int} determines the overall common mode noise performance. The typical value for the other coupling capacitances but the inter-winding capacitance falls into the range from 100 pF to tens of micro farads [9]. If C_{int} can be made much smaller than the other coupling capacitances, then the overall circuit input-to-output capacitance is governed by C_{int}.

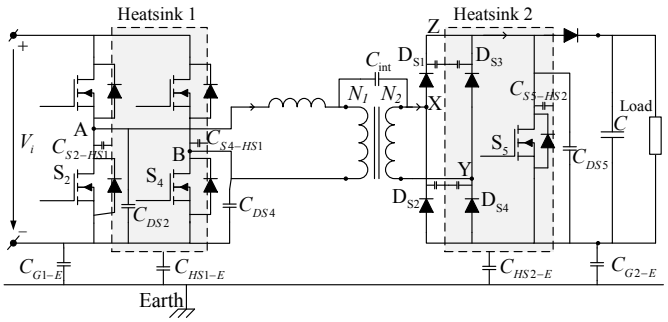


Fig. 2. Common mode noise paths

4 Transformer specification, configuration and validation

The proposed transformer's general structure is illustrated in Fig. 3a, whereas the transformer under test's photo is in Fig. 3b. In its winding configuration, the winding that has smaller number of turns will be place in the geometry centre of the core, forming a rectangular frame symmetrically around the core. The remaining winding with most number of turns is wounded tightly around the core. This is respectively the case of the secondary winding and primary winding in Fig. 3. With this structure, the two winding are separated from each other by a reasonably high distance. Moreover, the die-electric material between them is only the surrounding air, which has the second lowest permittivity to vacuum. All of these features results in an extremely low inter-winding parasitic capacitance that the transformer possesses.

To arrive at a design procedure or guideline of making a transformer that has a specific inter-winding parasitic capa-

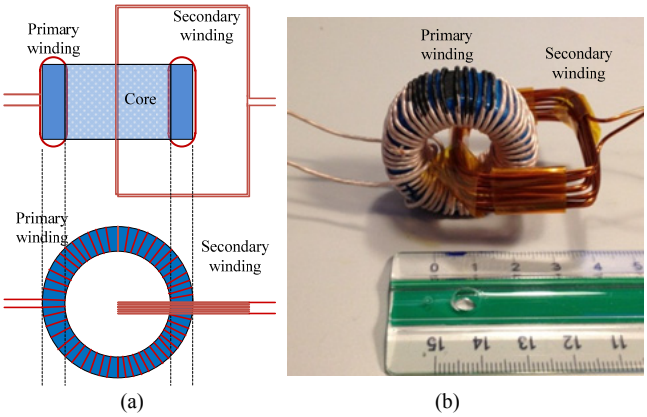


Fig. 3. Transformer structure: a) conceptual structure b) the transformer under test.

-citance, it usually requires mathematic modelling and solving, or simulation based on finite-element method. Apart from that, the design of the transformer is a compromise of different issues like its power losses and physical size of the whole circuit. The transformer is often the most bulky part in the prototype of a power electronics converter. As a result, the size of the transformer highly affects the size of the prototype. It is preferable to go for smaller size of transformer so that the prototype is smaller, and therefore, the parasitic capacitance coupling to earth is smaller. The derivation of the transformer design procedure can be treated as a separated issue. This issue, however, is not addressed in this paper, which focuses on system analysis and experiment validation of the converter as a whole.

Material	N87
Dimension	36 mm×25 mm×13 mm
Turn ratio	55:11
Primary winding	Litz-wire 60×0.2 mm
Secondary winding	Copper 1 mm

Table 2. Transformer parameters

The specifications of the developed transformer are provided in Table 2. Fig. 4. shows the experimental data of the inter-winding impedance magnitude and phase of the transformer. It is done with both terminals of each winding shorted. As can be seen, the impedance magnitude has a constant slope with -20dB/dec roll off, and the phase is around -90^0. Therefore, the inter-winding is capacitive and it is appropriate to model the inter-winding impedance as a lump-element circuit with an inter-winding-capacitor. The measured data are in the form of digital values of impedance's magnitude and phase at a sweep of different frequencies. They are imported into MATLAB and processed by proper scripts to yield the interpreted coupling capacitance, whose values are shown in Fig. 5. It can be seen that the capacitance value is around 10 pF in the wide range of frequency from dc to 10 MHz. It is validated that with the distinct configuration of the transformer, an extremely low inter-winding parasitic capacitance can be achieved.

The process is repeated for the measurement of the impedance between two terminals of the primary side while the two terminals of the secondary side shorted. This impedance can be modelled as a leakage inductor. The impedance magnitude and phase are shown in Figs. 6a and 6b. The impedance behaves like a resistor at frequency up to 1 kHz due to winding ohmic resistance, like a leakage inductor from 2 kHz to 1.5 MHz due to leakage flux, and like a capacitor from above 1.5 MHz due to the self-capacitance of the leakage inductor. The interpreted magnitude of the leakage inductor is shown in Fig. 6c. The leakage inductance value is 170 uH in the range of 100 kHz to 300 kHz. The consequential relatively high leakage inductance can be explained as being caused by the high geometry separation of the two windings which produces relatively large leakage flux outside the core. Hence, the proposed topology as well as its associated control approach should be able to utilize the leakage inductor. The control approach will be presented in the next section.

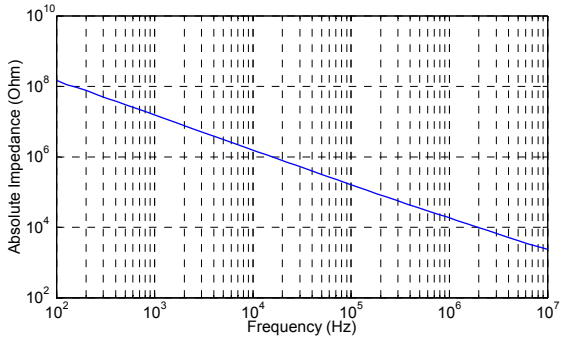


Fig. 4 (a)

Fig. 4(b)

Fig. 4. Inter-winding impedance measurement: a) magnitude, b) phase

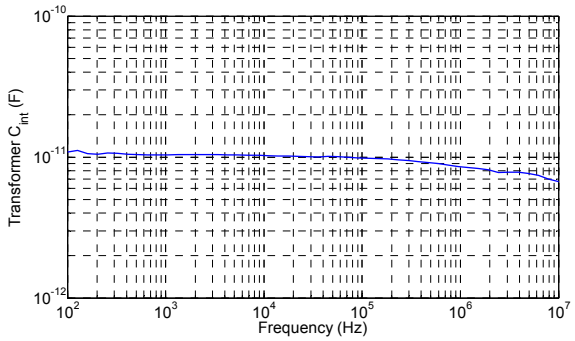


Fig. 5. Interpreted parasitic capacitance

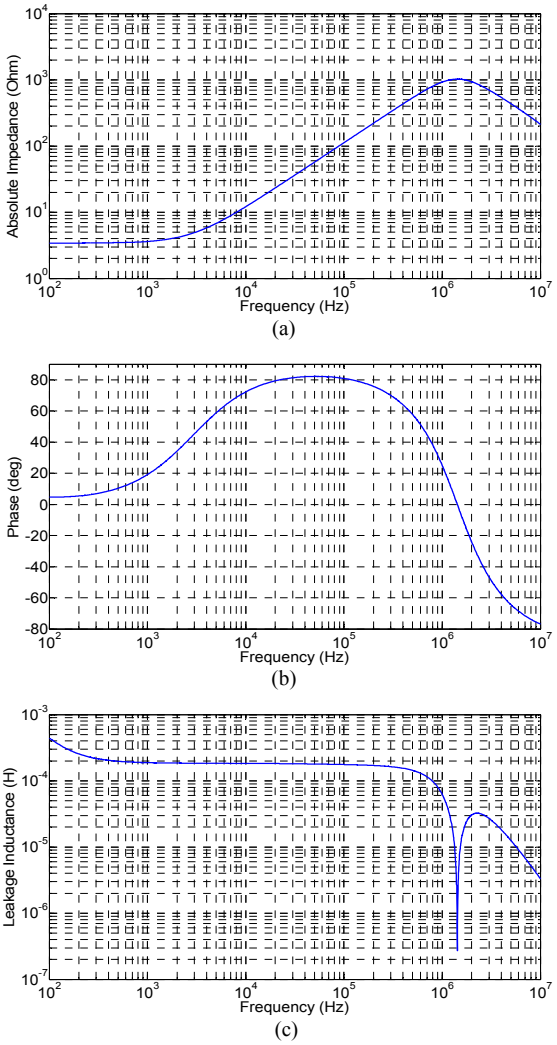


Fig. 6. Primary winding impedance: a) magnitude, b) phase, c) interpreted leakage inductance

5 Converter operation and control

In this paper, the control approach without an isolated feedback is adopted as to achieve minimum circuit input-to-output parasitic capacitance. The proposed physical configuration of the converter is shown in Fig. 7. There are two control loops where one resides in the primary and the other one resides in the secondary. The secondary side controller regulates the output voltage to be constant at 60 V. The primary side controller controls the primary-side inductor current; thus, indirectly regulate the nominal output current. The secondary side circuit can be seen as a current source supplying the output capacitor in parallel with the load. Because of the diode rectification in the secondary side, the output current is the result of the rectified inductor current multiplying with the inversion of the turn ratio.

$$I_S(t) = \frac{N_1}{N_2}\left|i_L(t)\right| \tag{1}$$

The secondary side controller regulates the output voltage to be constant at 60 V. The output voltage is sensed by a voltage divider, compared to a hysteresis reference to switch on and off the shunt switch S_5. When switch S_5 is on, shunting the

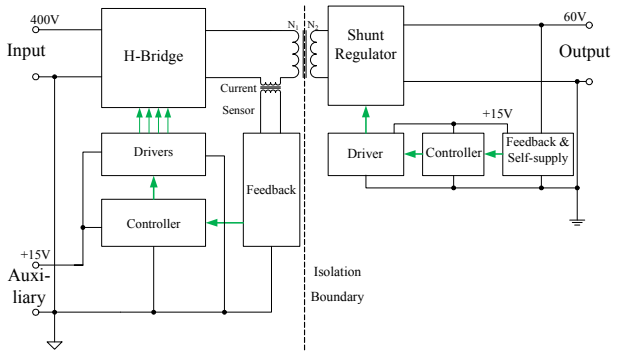
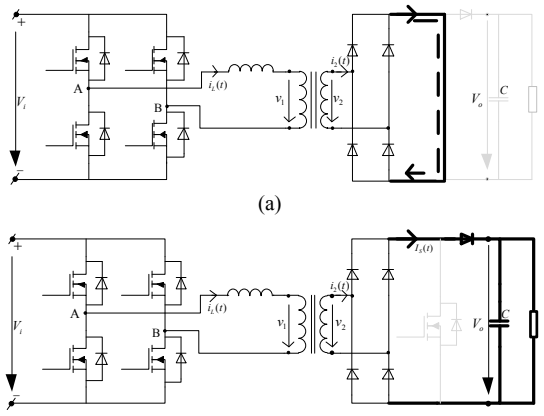


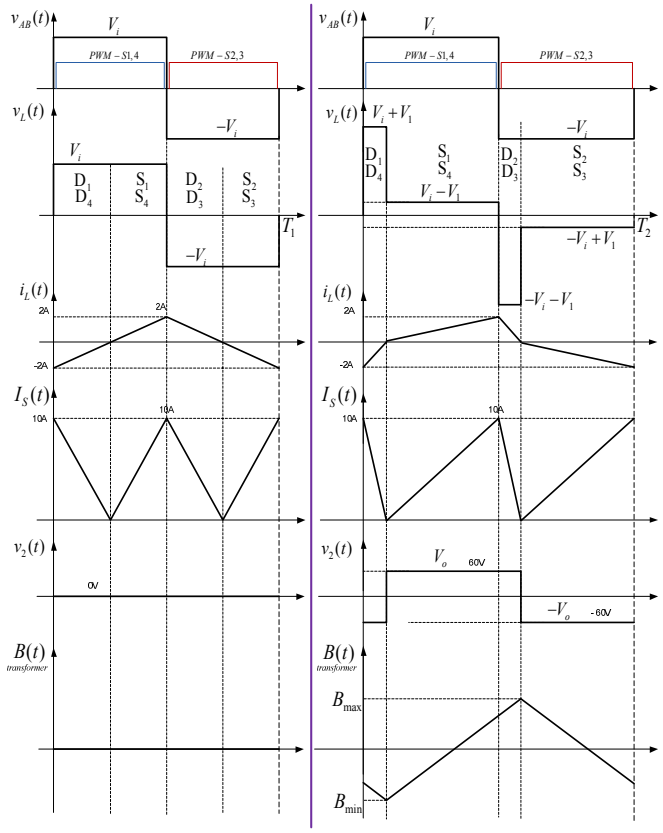
Fig. 7. Block diagram of the physical layout of the converter



(a)

(b)

Fig. 8. Operation modes: a) shunt mode, b) power mode.



(a) (b)

Fig. 9. Analytical waveforms when converter operates in a) shunt mode, b) power mode.

secondary side, the converter operates in its shunt mode (Figs. 8a and 9a); the output voltage decreases. Vice versa, when S_5 is off, the converter operates in its power mode, which is shown in Figs. 8b and 9b; the output voltage increases. In the primary side, since the leakage inductance is relatively high, which is 170 uH; it is utilized as the main inductor in the circuit and there is no external inductor added. The primary side inductor current can be controlled by either adjusting one variable among the three variables of the primary switches: frequency, phase shift, or duty cycle. In this paper, the frequency modulation is chosen. The duty cycle of the switches is kept at 50%, and the phase-shift is therefore at zero degree. The primary side current i_L is sensed and rectified. After that, it is low-pass filtered (LPF) to get the rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analogue proportional-integral (PI) compensator. The output of the PI compensator is fed to a voltage-controlled oscillator (VCO) to keep the rectified primary dc current to be constant at 1 A dc. With a turn ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc. The control block diagrams are presented in Fig. 10.

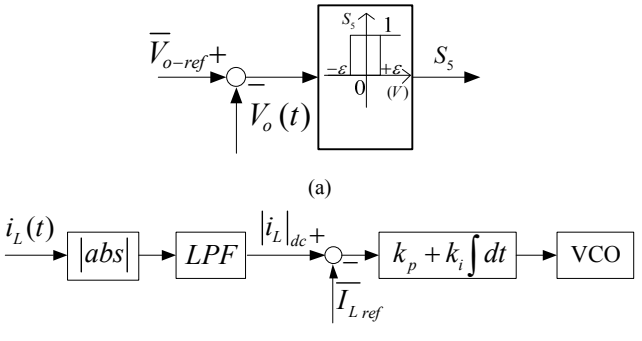
The switching frequency that ensure the primary side to be regulated at the peak value of $\hat{i}_L$ can be derived by equating the product of voltage across the inductor and time when the current is negative to the one during which the current is positive. It can be proved that:

$$f = \frac{V_i}{4\hat{i}_L L}\left(1-\frac{V_1^2}{V_i^2}\right) \tag{2}$$

In the power mode, the voltage across the primary winding of the transformer V_1 is reflected from the output voltage from the secondary side multiplied by the turn ratio if forward voltage drops from the rectifier stage diodes are neglected. In the shunt mode, this voltage becomes zero. As a result, the two switching frequencies at power mode and shunt mode are:

$$f_{power} = \frac{V_i}{4\hat{i}_L L}\left(1-\frac{(N_2V_0/N_1)^2}{V_i^2}\right) \tag{3}$$

$$f_{shunt} = \frac{V_i}{4\hat{i}_L L} \tag{4}$$



(a)

(b)

Fig. 10. Control block diagram: a) hysteresis control in the secondary side b) average current control in the primary side

6 Experimental results

6.1 Circuit input-to-output parasitic capacitance

The circuit input-to-output is measured with instrument Agilent 4294A precision impedance analyzer. The accuracy claimed is ±3% in the measured range. The two input terminals are shorted; and so do the two output terminals. Then the ground planes of the primary side and secondary side are measured with the instrument. Fig. 11 shows the circuit input-to-output impedance magnitude and phase measurement data. Its magnitude slope of -20db/dec and a phase around -90^0 makes it appropriate to be modeled as a capacitor. The measured value of the capacitance is around 10 pF, which is shown in Fig. 12. In short, an extremely low value of circuit input-to-output capacitance is achieved and it is proved to be dominated by the inter-winding parasitic capacitance.

6.2 Converter's transient response

In this section, two key measurement waveforms are presented and discussed. They are the leakage inductor current in the primary side and the output voltage in the secondary side. The measurement of the inductor current is performed with LeCroy AP015 current probe, which has a claimed accuracy of ±1%. In addition, the measurement of the output voltage is done with SI-9000 differential probe with a claimed accuracy of ±2%.

Fig. 13 shows the transient response from power mode to shunt mode, whereas the transient from shunt mode to power mode is shown in Fig. 14. The value of threshold ε is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady state values, which are 2 A peak and 60 V dc, respectively. The transient of the inductor current from power mode to shunt mode and vice versa finishes within about 30 us and 40 us, respectively. The time needed for the inductor current to settle is due to the dynamic of the average current control scheme described in Fig. 10b. Nevertheless, the transient and steady state are both stable and satisfactory, and the behavior of the circuit matches accurately with the aforementioned circuit analysis.

6.3 Converter's power efficiency

The power measurement is done with instrument PPA5530 precision power analyzer. The accuracy claimed by the manufacturer is ±0.4% in the operation condition under test. The measured efficiency as well as the calculated value at different power output is shown in Fig. 15. At the nominal output of 300 W, the converter operates entirely in its power mode. The switching frequency in the primary side is then the smaller one f_{power}. Therefore, primary switching loss, shunt MOSFET S_5 conduction loss and switching loss are reduced. That's the reason why peak efficiency is attained at the no-

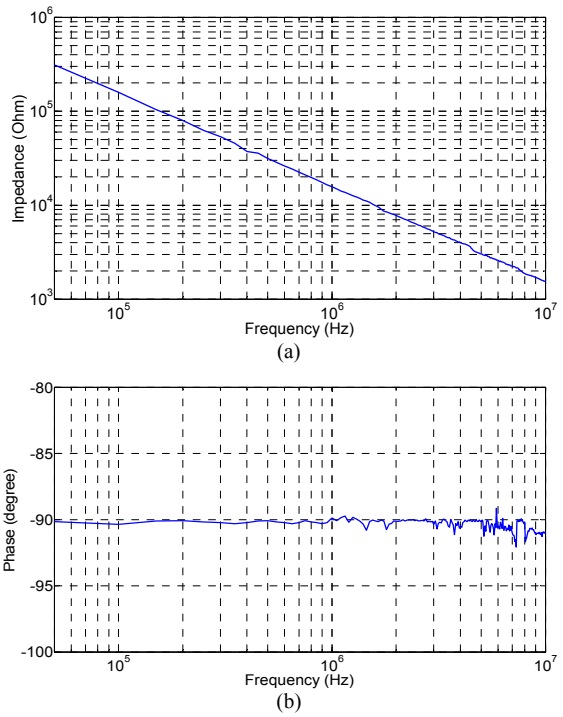


Fig. 11. Circuit input-to-output impedance measurement a) magnitude b) phase

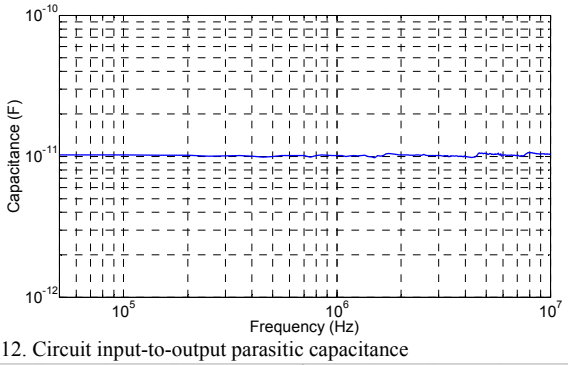


Fig. 12. Circuit input-to-output parasitic capacitance

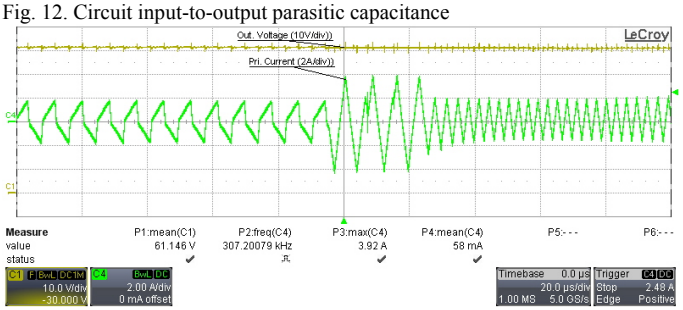


Fig. 13. Transient response from power mode to shunt mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div)

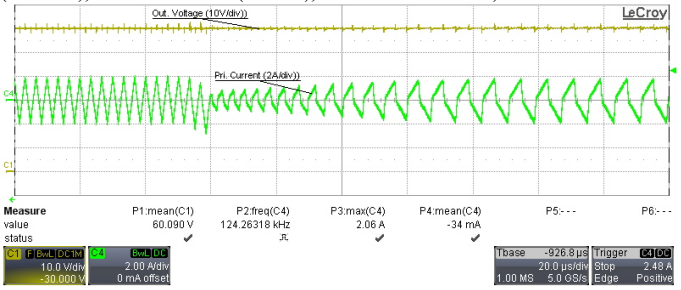


Fig. 14. Transient response from shunt mode to power mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div)

minal output power. This value is 92.4 %. As output power reduces, the duration in which the converter operates in shunt mode increases linearly; the loss increases slightly as shown in Fig. 16. Thus, the efficiency drops. Zero efficiency is attained at zero output power when the converter fully operates in its shunt mode. In general, the overall efficiency of the converter is satisfactory particularly in the range of 1/3 of the nominal power to the nominal power. The efficiency in this range is from 77.5 % to 92.4 %.

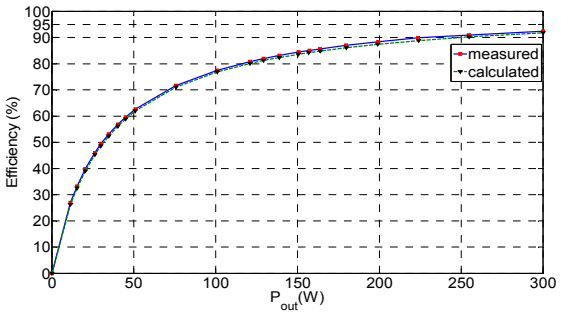


Fig. 15. Converter's power efficiency

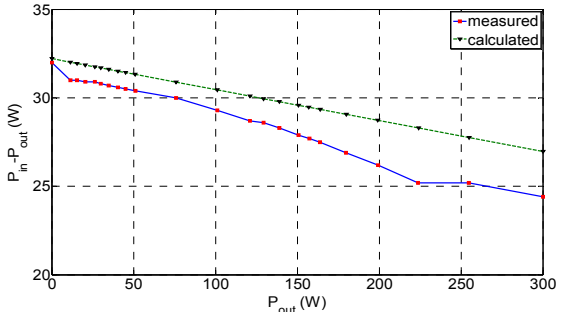


Fig. 16. Converter's power loss

7 Discussion

The several advantages of the developed converter's prototype are as follows. First, the topology and its control allow zero voltage switching at the turn on transitions of the switches (refer to Fig. 9). Second, this topology has higher power (60V/300W) per channel compared to 36V/5W of prior art with a similar topology. This allows the converter to be capable of supplying wider range of load, from 0 to 60 V and up to 5 A. Third, the achieved circuit input-to-output capacitance is extremely low of 10 pF. This is claimed based on observation that existing transformers in the literature, for example, in a 1.2 kW converter was reported to have 1.5 nF inter-winding capacitance [9], and an E-core transformer used in fly-back converter with a power rating of 30 W was reported in [10] to have 34 pF of inter-winding capacitance. Finally, the topology and its control allow zero output voltage and zero output power.

There are two main disadvantages of the topology. First, the MOSFETs at the primary side turn off at their peak currents, which results in higher turn-off loss. Second, the slightly increased loss at lighter load makes the converter's efficiency relatively low at low output power. Solutions might include the use of synchronous rectifier stage in the secondary side to reduce the loss.

8 Conclusion

In this paper, the authors have presented the design of a 300 Watt isolated power supply. The main advantage of the power supply is to have an extremely low inter-winding capacitance in the transformer, making the circuit input-to-output capacitance ultra-low considering its output power. Circuit operation and control have been demonstrated and experimental data are also provided, that proved to match well with expectations. Furthermore, the advantages as well as the disadvantages of the converter are also discussed. In summary, the converter is suitable for a wide range of power supply applications and especially for modular stacking applications, where minimization of the circuit input-to-output capacitance is vital.

References

[1] M. A. E. Andersen, "MOS Gate Driver Circuit with Extremely High Galvanic Isolation", EPE 1995. Sevilla, Spain, vol. 1, p. 747,751.

[2] "Auxiliary Power Supplies for Medium and High Voltage Applications", Bodo's Power System, July 2012

[3] "Power Electronics for Medium-Voltage Applications", Bodo's Power System, March 2013

[4] "Interlink coupling high-voltage impact isolation transformer," May 12 1999, CN Patent 2,318,700. [Online]. Available: https://www.google.com/patents/CN2318700Y?cl=en

[5] S. Wang , P. Kong and F. C. Lee "Common mode noise reduction for boost converters using general balance technique", IEEE Trans. Power Electron., vol. 22, no. 4, pp.1410 -1416, Jul. 2007

[6] Pengju Kong; Lee, F.C., "Transformer structure and its effects on common mode EMI noise in isolated power converters," Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, pp.1424,1429, 21-25 Feb. 2010

[7] Nakao, Hiroshi; Yonezawa, Yu; Nakashima, Yoshiyasu; Sugimoto, Toshio; Horie, Takeshi, "Soft switching for power factor correction for server power supply unit," Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference, pp.1,4, 27-29 March 2012

[8] Meisser, M.; Haehre, K.; Kling, R., "Impedance characterization of high frequency power electronic circuits," Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference, pp.1,6, 27-29 March 2012

[9] M. Borage, S. Tiwari, S. Kotaiah, "Common-mode noise source and its passive cancellation in full-bridge resonant converter," *Electromagnetic Interference and Compatibility, 2003. INCEMIC 2003. 8th International Conference on* , pp.9-14, 18-19 Dec. 2003

[10] D. Garabandic, D. W.G. Dunford, M. Edmunds, "Zero-voltage-zero-current switching in high-output-voltage full bridge PWM converters using the interwinding capacitance," IEEE Trans. Power Electron., vol.14, no.2, pp.343,349, Mar 1999

A.3 (IEEE-TPEL JOURNAL)-Design of a 300-W Isolated Power Supply for Ultrafast Tracking Converters

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Design of a 300-W Isolated Power Supply for Ultrafast Tracking Converters

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***Abstract*—This paper presents the design of a medium-power-rating isolated power supply for ultrafast tracking converters and MOS-gate driver circuits in medium- and high-voltage applications. The key feature of the design is its very low circuit input-to-output parasitic capacitance, which maximizes its immunity from noise due to fast changes in voltage. The converter is a voltage-controlled current source, utilizing a transformer with extremely low interwinding parasitic capacitance, which is achieved by separating the windings by a significant distance. Experimental measurements show that an overall circuit input-to-output parasitic capacitance of 10 pF in a 300-W prototype can be achieved. The circuit input-to-output capacitance per watt is therefore 30 times lower than that of existing approaches. A mathematical model of the interwinding capacitance of the proposed transformer, circuit analysis, and experimental results are provided to prove the feasibility of the converter.**

***Index Terms*—Current transformers, dc–dc power converters, parasitic capacitance, stacking, switching converters.**

I. Introduction

COMMON mode (CM) noise is a typical problem in most switching power electronics converters and is well known to cause various adverse effects. Among them are electromagnetic interference, false measurements, and unexpected triggering of sensitive control electronics. In particular, the problem becomes more severe where modular stacking of converters is used to increase the total power rating, as the total CM noise may add up, change the output impedance, or resonate in different coupling paths [1], [2]. As a result, many studies have been dedicated to mitigate CM noise generated by power electronics converters [1]–[5].

CM noise occurs due to different sources and coupling through different paths. Among them, CM noise current exists when there are switching nodes with stiff changes of voltage over time (high *dv/dt*), and when there are capacitive coupling paths. Unfortunately, high *dv/dt* switching nodes are inherent in most switching converters and are unavoidable. Due to the use of more advanced power switches capable of switching at higher frequency for a higher efficiency, CM noise has become more notable. As a result, one of the common approaches to reduce effects of CM noise current is to improve the capacitive coupling paths.

In [4] and [5], a method called current balancing technique is proposed to cancel the CM noise for several nonisolated converters. For example, in [4], analysis is performed on the boost converter, where different equivalent circuits for CM sources are drawn, and the major main noise source is identified. After that, circuit modification, mainly with the insertion of an extra capacitor and splitting of the main inductor are suggested, so that the resulting generated CM currents cancel out the original CM current on the line impedance stabilization network [6].

In most galvanic isolated converter topologies that utilize a transformer, the CM noise couples through the interwinding parasitic capacitance of the transformer. Their coupling paths may also include the parasitic capacitances from the converter chassis to ground, or from the drain of the converter switches to heat sink and from heat sink to ground. If a proper design is achieved to minimize most of these parasitic capacitances due to circuit structure, the element that predominantly contributes to the circuit total input-to-output parasitic capacitance is the transformer [1]–[5]. Therefore, many studies have focused on mitigating CM noise by minimizing the interwinding capacitance of the transformer [1], [2], [7]–[9], compensating the noise generated by the converters [8], [10], or inserting line filters [11]. The existing transformers in medium-power converters (up to 1.2 kW) have their interwinding capacitance in the range of several tens of picofarads for low-output power converters to hundreds of nanofarads for higher power ratings. For example, the existing transformer in a 1.2-kW converter is reported to have 1.5-nF interwinding capacitance [12]. An E-core transformer used in a flyback converter with a power rating of 30 W is reported to have 34 pF of interwinding capacitance [13]. The interwinding capacitance per unit output power is approximately 1 pF/W. The question, however, is how to further minimize the interwinding capacitance of the transformer in order to reduce the effect of the CM noise.

In [1], a novel converter topology supplying energy to MOS-gate driver circuits [e.g., MOSFETs, insulated-gate bipolar transistor (IGBT)s or MOS-controlled thyristor (MCT)s] is proposed that possesses a very low circuit input-to-output parasitic capacitance. The topology is redrawn in Fig. 1. In that topology, a unique structured ring core current transformer is used, where the primary winding is placed in the center of the ring,

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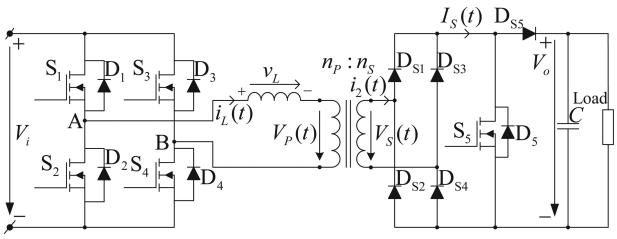

Fig. 1. Topology of the proposed converter.

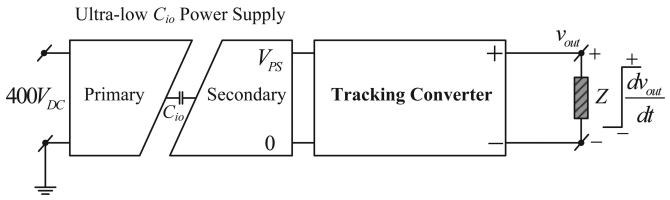

Fig. 2. Example of the proposed ultralow circuit input-to-output capacitance power supply connected with an ultrafast tracking converter.

TABLE I
DESIGN SPECIFICATION

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Circuit input-to-output capacitance	10 pF

displacing with the secondary winding a distance equal to the radius of the core. With this special structure, the distance between windings is maximized; therefore, the parasitic capacitance between them is minimized. An R25/10 toroid ferrite core with one primary winding and a 30-turn secondary winding was claimed to achieve as low as 1 pF of parasitic capacitance. The application is primarily to supply energy to MOS-gate driver circuits. Particularly, the purpose is to drive 15 gate driver circuits, with a full output voltage of 36 V and a current supply per channel of 0.2 A. Following this proposal, similar ideas of using the ring core transformer with that unique winding structure have been reported [3], [14]. In [3], the ring core transformer is used as a current loop to provide isolation and energy to supply gate drivers of power switches in medium-voltage applications of up to 16 kV dc. Specifically, 12 channels are stacked in parallel to provide output voltage adaptation for the IGBT driver boards. The power rating is 75 W per channel.

Despite being very promising, works in [1], [3], and [14] lack supporting experimental results from the ideas proposed. As a result, further work should be carried out to verify the ideas and improve the work. First, a detailed analysis and calculation on the transformer design are greatly desired, of which the results should indicate how to further improve the transformer in terms of minimizing the interwinding capacitance. Second, the power rating of the converter, which was 36 V and 0.2 A per channel as in [1], can be increased if applications require. Third, the work can be improved with elaborate circuit operation analysis and control together with presentation of supporting experimental data. Finally, it would be much appreciated if proper assessments of advantages as well as disadvantages of the converter were made.

This paper seeks to further investigate and validate the merit of the converter shown in Fig. 1. A higher output power rating is desired (300 W per module). The prototype is designed in a way that minimizes the circuit input-to-output parasitic capacitance, making it less susceptible to high *dv/dt* noise and therefore suitable for modular stacking. The paper is divided into the following sections. The first section is the introduction. Section II provides information on the system specification. Following that, Section III presents the targeted applications and selection of a suitable topology. Next, the CM noise current paths are briefly discussed in Section IV. Afterward, Section V discusses the design and specification of the proposed toroidal transformer. Mathematical expressions of the transformer interwinding capacitance are derived based on the method of stored energy balancing. The results indicate how to further improve the design in terms of minimizing the interwinding capacitance. Following that, Section VI discusses the circuit operation and control approach in detail. Section VII presents and examines the experimental results. Section VIII is dedicated to an overall discussion, where the advantages as well as disadvantages of the proposed converter are assessed. Finally, Section IX summarizes the contributions. The experimental results show that an overall circuit input-to-output parasitic capacitance of 10 pF is achieved. To the authors' best knowledge, this is the lowest circuit input-to-output parasitic capacitance achieved among similar devices with similar power ratings. It is also experimentally verified that the main contributor to the overall circuit input-to-output parasitic capacitance is the interwinding capacitance of the transformer.

II. SYSTEM DESCRIPTION

Referring to the converter in Fig. 1, the input dc supply voltage of the converter is usually the output of a power factor correction converter which converts a single phase 220-V ac voltage into 400-V dc voltage. Therefore, a dc input of 400 V is chosen in the design. The output voltage is chosen to be 60 V dc, since it allows a variety of power switch selections which have a breakdown voltage of 100 V. If, for example, higher output voltage is desired, then either design specification can be changed or multiple converter modules can be stacked in series. The output current is designed to be 5 A average value at its maximum. This specification implies that the maximum output power that is available in the output terminals is 300 W. Furthermore, an extremely low total circuit input-to-output parasitic capacitance of 10 pF is sought. All of these specifications are stated in Table I.

III. TARGETED APPLICATIONS AND SELECTION OF TOPOLOGIES

A. Targeted Applications

One of the primary applications of this study is supplying energy for ultrafast tracking converters. Fig. 2 shows a configuration in which a module of the proposed power supply provides

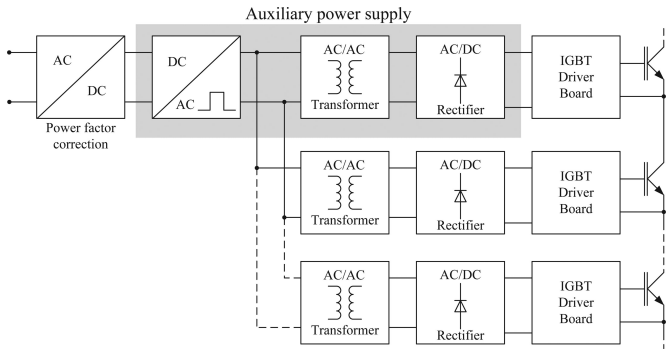

Fig. 3. Auxiliary power supply for MOS-gate driver circuits in medium- and high-voltage application [15].

energy to a module of an ultrafast tracking converter. An ultrafast tracking converter is typical of radio frequency power amplifiers used in communication system based stations [16]–[18]. The output voltage of such an ultrafast tracking converter can be required to have a step response settled within 10 μs. Due to the high *dv/dt* at the output of the tracking converters, there will be a large amount of conductive CM current drawn from their output. This current is linearly proportional to the input–output capacitance of the power supply

$$i_{\rm com} = C_{io}\frac{dv_{\rm out}}{dt}. \tag{1}$$

However, the ripple voltage requirement of the output of the tracking converter is usually in the range of tens of millivolts peak to peak; for example, 10 mV as in [16] and [17]. The performance of the tracking converter can be degraded if a reasonable amount of conductive current is drawn from the output through the circuit input-to-output capacitance. The adverse effects become worse if there are more than one converter stacked together to increase the power rating. Therefore, in order to have high immunity to the fast voltage step response, the circuit input-to-output parasitic capacitance must be minimized, especially in the modular stacking applications.

Another important application of this study is to power the gate-drive circuits of medium- and high-voltage applications. Existing approaches can be found in [3], [15], and [19]. The medium- and high-voltage applications are defined as applications with operating voltage in the range of tens of kilovolts. For example, a high-speed IGBT switch which acts as a circuit breaker for the operating voltage of 16 kV dc and a permanent load current of 10 A dc is demonstrated [15]. This is performed by connecting in series a total of 18 IGBTs, each with a reverse voltage of 2500 V. Each IGBT has its own attached gate drive circuit, all of which were driven by a single auxiliary power supply unit. The block diagram of this system is redrawn and shown in Fig. 3. According to [15], the following features of the auxiliary power supply unit that generates the control power required to activate the high-power IGBT switches are required:

1) Insulation between individual stages and with respect to earth potential.
2) A small coupling capacitance in order to achieve a high level of noise immunity between the individual stages.

In [3], [15], and [19], it is shown that the auxiliary power supply should be implemented in the form of a current loop shared by all switch stages. The current loop provides power to a gate drive circuit by using a ring core transformer. This results in a solution with low coupling capacitance and compact construction volume [15].

A small coupling capacitance of the power supply circuit can make the converter highly immune to high *dv/dt* and thus increase reliability in such applications. The main focus of this paper is to develop a converter that has minimized circuit input-to-output capacitance for applications that require high immunity to a large change of output voltage over time.

B. Effect of Isolated Feedback to the Circuit Performance

In consideration of feedback control applied to isolated power converters, it is very common to feedback signals from one side of the circuit to the other side across the isolation boundary. The feedback elements must provide electrical isolation to the control feedback paths; at the same time, they must be able to transfer information as quickly and accurately as possible. Examples of such elements are optocouplers and signal-level isolation transformers. However, these components possess several undesirable attributes that need to be taken into account.

For the optocoupler, there are two main disadvantages. First, they have very low bandwidth and limited accuracy that lower the converter's overall bandwidth and might inhibit fault protection of the circuit. This is due to the fact that the optocoupler must have large based region in order to be sensitive to light and have very thick based region in order to minimize the losses in radiant energy transfer, which implies a relatively large Miller capacitance in the range of nanofarads [20]. This large capacitance effectively reduces the bandwidth of the optocoupler. The typical value of the bandwidth of a commercially available optocoupler used in power supplies is less than 5 kHz [20].

Second, the input–output coupling capacitance inherent in an optocoupler will add to the overall circuit input-to-output parasitic capacitance. Therefore, an optocoupler is not a suitable candidate for the targeted applications. Signal-level isolation transformers have better bandwidth than the optocoupler, but they have higher coupling capacitance. The typical coupling capacitance of a signal-level transformer is from 2 pF [21] to 12 pF [22], which will add 20% and 120% to the total circuit input-to-output capacitance, respectively. Hence, the use of an isolation transformer in feedback is not acceptable in such applications.

In summary, the control approach which uses feedback paths across the isolation boundary is not optimal where minimization of circuit input-to-output parasitic capacitance is the primary goal. Next, the selection of a suitable topology will be discussed.

C. Topology Selection

Based on the targeted applications and the awareness of the effect of isolated feedback on the circuit performance, a power supply suitable for these applications must possess the following features:

1) Low circuit input–output capacitance.
2) Reduced number of crossings of the isolation barrier.

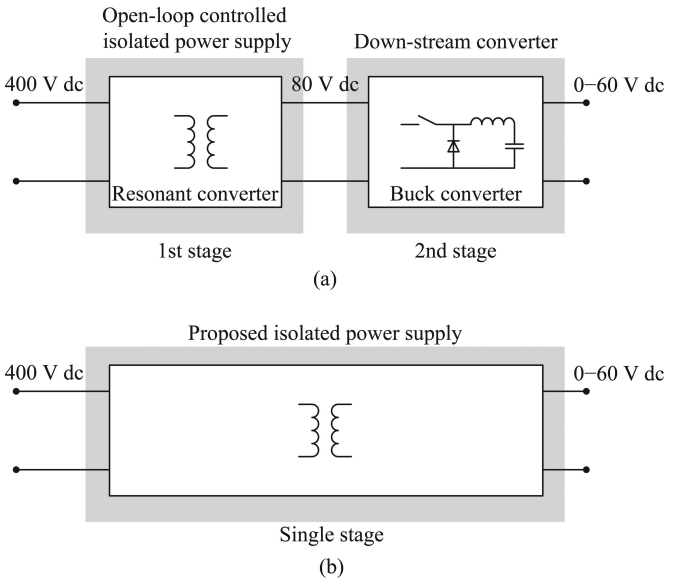

Fig. 4. Minimized circuit input–output capacitance systems: a) Two-stage solution with existing topologies, b) one-stage solution with the proposed topology.

The first requirement implies a loosely coupled transformer to be used. However, one property of the magnetic component to be noted is that the leakage inductance and the interwinding parasitic capacitance are inversely proportional to each other [23]. Taking this into account, it can be concluded that conventional full-bridge converters such as buck- or boost-derived converters are not suitable for these applications. This is because, in those topologies, the transformer requires low leakage inductance and consequently high interwinding capacitance due to the close proximity requirement between windings. This will increase the total circuit input–output capacitance. Furthermore, those topologies usually involve the use of feedback elements crossing the isolation boundary and thus violate the aforementioned second requirement.

The relatively high transformer leakage inductance due to the loose coupling can be useful in resonant topologies [24]–[26] This suggests an approach shown in Fig. 4(a), based on a two-stage converter. The configuration utilizes only standard existing topologies. The system is powered by a power factor correction whose output voltage is assumed to be 400 V dc. The resonant converter operates with open-loop control to eliminate the feedback from output to the input. Its output voltage is used to supply a nonisolated down-stream converter, such as a buck converter, as demonstrated in Fig. 4(a). The closed-loop regulation of the final output voltage is performed by the down-stream converter, while the low circuit input-to-output capacitance is determined by the loose coupling and feedback-free operation of the resonant converter. For example, if the down-stream buck converter has a maximum output voltage level of 60 V, then the resonant converter can be designed for a voltage output of about 80 V. In short, in order to attain the two aforementioned goals, it must be done with a two-stage converter with a separate control loop for each stage. This approach, however, can be costly and require significant effort to develop a separate control loop for each stage.

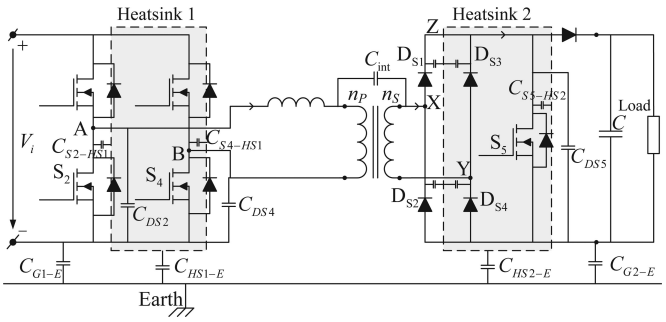

Fig. 5. CM noise paths.

Considering the control performance, a feedback-free resonant converter design is only optimal if the switching frequency is fixed at the load-independent frequency, where the converter gain is independent of variation in the load. However, this creates disadvantages if the open-loop control fails to track the load-independent point due to the tolerances of the control and sensing circuits as well as of the power circuit. The variation of the voltage gain around the vicinity of the load-independent point can cause the voltage to fail. Moreover, the regulation of the down-stream converter speed is limited by the output filter used.

This paper proposes a converter and control that combine two stages into one stage. The concept is shown in Fig. 4(b). The proposed converter and its control is free from feedback across the isolation boundary. However, the output voltage is locally controlled by a closed loop in the secondary side, and thus, it maintains the high performance and robustness against the control circuit tolerance and circuit parameter variation. The transformer structure, modeling, and validation will be presented in Section V. The detailed analysis of the control approach will be presented in Section VI.

IV. CM Noise Current Paths

To better understand the effect of the difference coupling capacitance to the overall circuit input-to-output capacitance, the CM noise current paths are studied in this section.

The CM noise paths are shown in Fig. 5. In this topology, the nodes that have high *dv/dt* are nodes A, B, X, Y, and Z. In nodes A and B, there are changes of voltage from $\pm V_i$ to $\mp V_i$ with respect to the primary-side return. Nodes X, Y, Z see a change of 0 to 60 V with respect to the secondary-side return. These nodes are sources of CM noise currents. In the developed prototype, there are two heat sinks used, one for each side to reduce the capacitive coupling between the two sides. Since the drains of switch S_2 and S_4 are switching nodes and they are both attached to heat sink 1, the coupling paths include capacitances from the drains of S_2 and S_4 to heat sink 1, and capacitance from heat sink 1 to chassis/earth. In implementation, the heat sink can be electrically connected to the return path (not the chassis/earth) to further mitigate the transmission of CM noise current. The coupling paths in the secondary side include capacitances from cathodes of D_{S1}, D_{S2}, D_{S3}, D_{S4}, and the

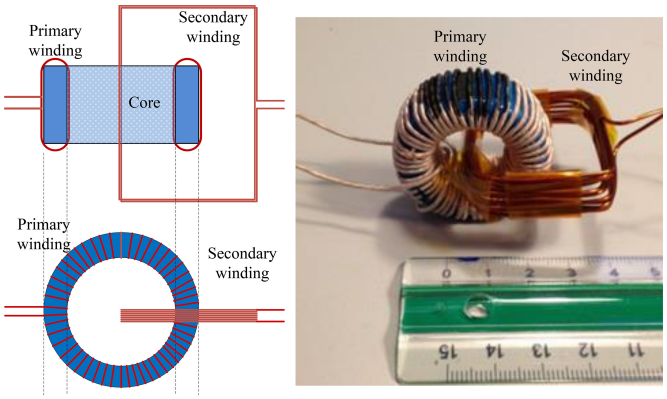

Fig. 6. Transformer structure. (a) Conceptual structure top and side view and (b) the transformer prototype.

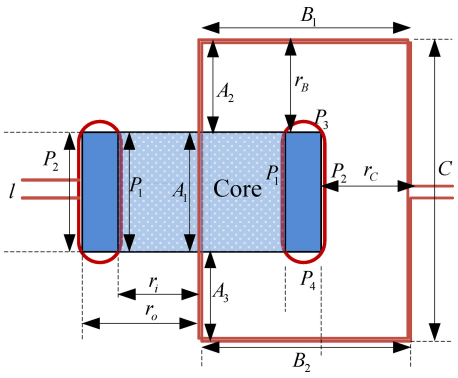

Fig. 7. Proposed transformer structure and geometry.

drain of S_5 to heat sink 2, and capacitance from heat sink 2 to chassis/earth. The coupling path caused by the transformer comes from the interwinding capacitance, $C_{\rm int}$. It can be clearly seen that $C_{\rm int}$ is in series with the other coupling capacitances, forming a loop of CM noise paths. Therefore, the value of $C_{\rm int}$ determines the overall CM noise performance [27]. The typical value of the other coupling capacitance falls into a range from 100 pF to tens of microfarads [2], [12], [13]. If $C_{\rm int}$ can be made much smaller than the other coupling capacitances, the overall circuit input-to-output capacitance will be governed by only $C_{\rm int}$.

V. Transformer Structure, Interwinding Capacitance Modeling, and Validation

In this section, the transformer structure, its specification, and its interwinding capacitance mathematical model will be presented first. After that, key measurement data including the transformer's primary to secondary winding impedance, the interpreted transformer's interwinding capacitance, and the leakage inductance referred to the primary side will be given.

A. Transformer Structure

The general structure of the proposed transformer is illustrated in Fig. 6(a), and the transformer prototype photo is shown in Fig. 6(b). In its winding configuration, the winding with fewer turns will be placed in the geometrical center of the core, forming a rectangular frame. The remaining winding with more turns is tightly wound around the core. This is, respectively, the case of the secondary winding and primary winding in Fig. 6. With this structure, the two windings are separated from each other by a reasonably large distance. Moreover, the dielectric material between them is only the surrounding air that has the second lowest permittivity to vacuum. All of these features result in the transformer's extremely low interwinding parasitic capacitance.

To arrive at a design procedure or guideline of making a transformer that has a specific interwinding parasitic capacitance, depending on how precise it is expected to be, this normally requires mathematical modeling or simulation based on the finite-element method (FEM). Apart from that, the design of the transformer is a compromise of other issues such as the power losses and physical size of the whole circuit. The transformer is often the most bulky part in the prototype of a power electronics converter. As a result, the size of the transformer greatly affects the size of the prototype. It is preferable to select as small a transformer size as possible so that the prototype is smaller; therefore, the parasitic capacitance coupling from the prototype to earth is smaller.

Transformer parasitic capacitance cannot be ignored. The voltage potential between turns, between winding layers, and between windings and the core create this parasitic element. In fact, this parasitic capacitance significantly affects the magnetic component performance, such that the current waveform on the excitation side would be distorted, and the overall efficiency of converters would be decreased. Subjected to high-voltage stresses, the interwinding capacitance causes leakage currents and consequently contributes to the EMI problem [28].

The specifications of the developed transformer are provided in Table II. It also provides dimensional information about the core and winding with respect to the notations in Fig. 7. It is an R36/23/15 toroid core from Epcos with N87 material. The primary winding is made by Litwize with 60 0.2-mm-diameter twisted parallel wires. The secondary winding uses copper wire with a 1-mm diameter. The turns ratio is 55:11.

The interwinding capacitance can be calculated by using the stored electric energy method [28]–[33], in which voltage distribution plays a vital role. The energy stored can be derived by either an FEM simulation model based on commercial software or a mathematical model. However, FEM has a particular disadvantage in deriving the interwinding capacitance of the proposed transformer. A 2-D FEM simulation model based on Ansoft/Maxwell software has been built to observe the energy stored in the transformer. Fig. 8 shows the result of the energy stored created by the segment of the secondary winding that is in the center of the core and the primary winding. Because the displacement distance between the secondary winding and the primary winding is large and the turn to turn distances of each winding are much smaller, the energies stored between turn to turn of the windings dominate the interwinding energies. The simulation result in Fig. 8 shows that the energy is concentrated

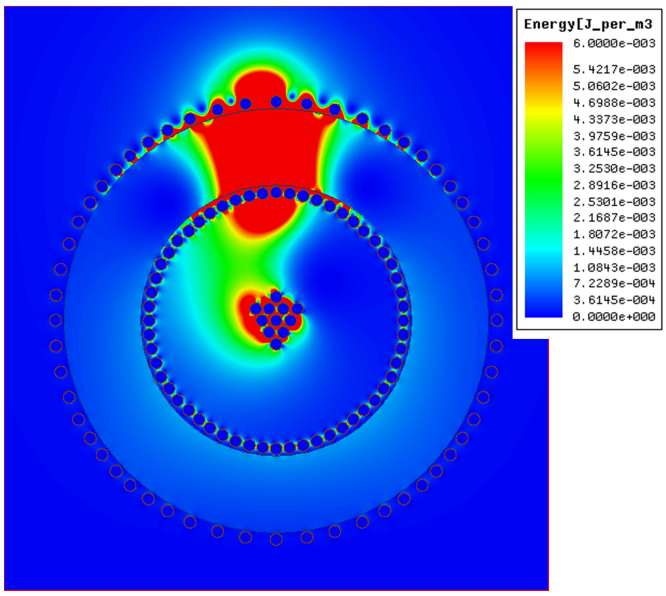

Fig. 8. 2D FEM simulation result of the winding energy distribution.

near the two ends of the primary winding. This is reasonable because in the proximity of the two ends, the voltage differences are maximum and the turn to turn displacements are minimum.

The two kinds of energy, turn-to-turn energy and interwinding energy, cannot be simulated separately with FEM software. This is one of the reasons why a mathematical model is adopted for this paper. The other reason to model the interwinding capacitance with mathematics is that it will allow fast recalculation with minor parameter modifications if a transformer with the same structure is used but possesses different geometry, turns ratio, and winding parameters. It, therefore, allows performance of an optimization routine of the transformer design.

The calculation based on a mathematical model will be presented next.

B. Mathematical Model of the Interwinding Capacitance

First, the interwinding capacitance caused by the interaction between segment A_1 of the secondary winding through the core center to the parallel segments P_1 and P_2 of the primary winding (see Fig. 7) will be calculated. Segments P_1 and P_2 are the winding segments around the perimeters of the inner ring and outer ring, respectively. The secondary winding has 11 turns stranded together, so each turn is located in the approximate center of the magnetic core, as shown in Fig. 6. The static capacitance between the inner primary turns and the secondary turns can be expressed as [28], [30]

$$C_i = \frac{\epsilon_0 S}{r_i} = \frac{\epsilon_0 d\pi l}{2r_i}, \tag{2}$$

where ϵ_0 is the permittivity of free air space, d is the diameter of each turn (the same size of wire is selected for both primary and secondary turns), and l and r_i are the overlapped length and the distance between the inner primary turns and the secondary turns, respectively.

With respect to the outer ring of the primary winding, the static capacitance can be expressed with a different distance r_o

$$C_o = \frac{\epsilon_0 S}{r_o} = \frac{\epsilon_0 d\pi l}{2r_o}. \tag{3}$$

Assuming that the voltage potential distribution along the primary winding varies linearly

$$V_P[i] = \frac{i}{n_p - 1} V_P \quad (i = 0, 1, 2, 3, \ldots, n_p - 1). \tag{4}$$

Then, the total stored electric energy between all secondary turns lying in segment A_1 and the inner ring of primary winding P_1 is

$$E_i = \frac{1}{2} C_i \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2. \tag{5}$$

With the same analytical approach, the total stored electric energy between all secondary turns and the outer ring of the primary winding P_2 can be expressed as

$$E_o = \frac{1}{2} C_o \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2. \tag{6}$$

The contribution of segment *B* of the secondary winding to the total energy is computed as follows. The capacitance caused by the side segments B_1 , B_2 to the primary winding is

$$C_B = \frac{\epsilon_0 d\pi l_B}{2r_B}. \tag{7}$$

Segments B_1 and B_2 face the middle parts of the primary winding. It is appropriate to assume that there are five turns from the primary winding that lie in segment P_3 or P_4 of Fig. 7 facing segment B_1 and B_2, respectively. They are turn number $(n_p - 1)/2 - 2$ to $(n_p - 1)/2 + 2$. In a specific design with 55 primary turns, these will correspond to turn number 25 to 29. Then, the stored electric energy caused by B_1 and B_2 is

$$E_B = 2 \left(\frac{1}{2} C_B \sum_{j=0}^{n_s-1} \sum_{i=(n_p-1)/2-2}^{(n_p-1)/2+2} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2 \right). \tag{8}$$

Next, the contribution of segment *C* of the secondary winding to the outer ring of the primary winding is computed. Referring to Fig. 9(c), it is helpful to mathematically express the distance from segment *C* to the turns lying in the outer ring of the primary. In triangle CDB, distance $\overline{\mathrm{CB}}$ is related to other sides of the triangle by

$$\begin{aligned} \overline{\mathrm{CB}}^2 &= \overline{\mathrm{CD}}^2 + \overline{\mathrm{BD}}^2 - 2\overline{\mathrm{CD}}\overline{\mathrm{BD}}\cos(\Phi) \\ &= (r_i + r_o)^2 + r_o^2 - 2(r_i + r_o) r_o \cos(\pi - 2\pi/n_p). \end{aligned} \tag{9}$$

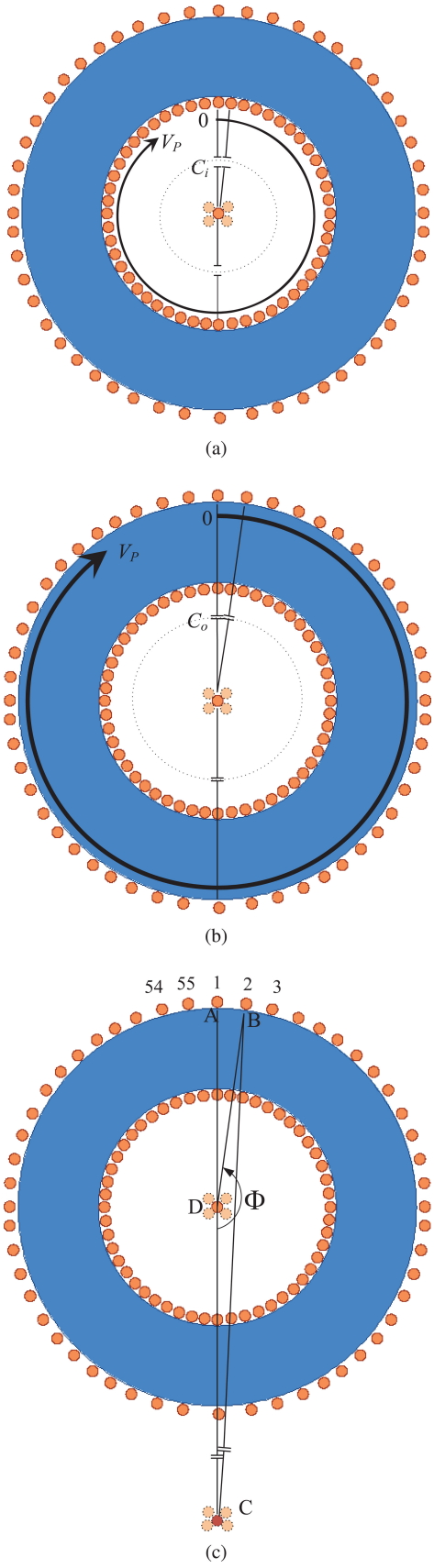

Fig. 9. Effect of parasitic capacitance from the secondary winding of (a) segment A to the inner ring of the primary winding, (b) segment A to the outer ring of the primary winding, and (c) segment C to the outer ring of the primary winding.

Therefore, the distances from C to the ith turn of the outer-primary winding are

$$r_{C\text{out},i} = \sqrt{(r_i + r_o)^2 + r_o^2 - 2(r_i + r_o) r_o \cos\left(\pi - \frac{i2\pi}{n_p}\right)} \quad (i = 1, 2, 3, ..., n_p - 1). \tag{10}$$

The capacitance from segment C of the secondary winding to turn number ith of the outer primary winding is

$$C_{C\text{out},i} = \frac{\epsilon_0 d\pi l_C}{2\sqrt{(r_i + r_o)^2 + r_o^2 - 2(r_i + r_o) r_o \cos\left(\pi - \frac{i2\pi}{n_p}\right)}} \quad (i = 1, 2, 3, ..., n_p - 1) \tag{11}$$

The total stored energy caused by segment C of secondary winding to the outer ring of primary winding is then

$$E_{C\text{out}} = \frac{1}{2} \sum_{j=0}^{n_s - 1} \sum_{i=0}^{n_p - 1} C_{C\text{out},i} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2. \tag{12}$$

Similarly, the stored energy caused by segment C of secondary winding to the inner ring of primary winding is

$$E_{C\text{in}} = \frac{1}{2} \sum_{j=0}^{n_s - 1} \sum_{i=0}^{n_p - 1} C_{C\text{in},i} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2, \tag{13}$$

where

$$C_{C\text{in},i} = \frac{\epsilon_0 d\pi l_C}{2\sqrt{(r_i + r_o)^2 + r_i^2 - 2(r_i + r_o) r_i \cos(\pi - \frac{i2\pi}{n_p})}} \quad (i = 1, 2, 3, ..., n_p - 1). \tag{14}$$

The total stored electric energy is then

$$\begin{aligned} E_{\text{total}} &= E_i + E_o + E_B + E_{C\text{in}} + E_{C\text{out}} \\ &= \frac{1}{2} C_{\text{int}} (V_P - V_S)^2. \end{aligned} \tag{15}$$

The calculated interwinding capacitance, C_{int}, based on the parameters in Table II is 10 pF. Table III shows the calculated energy and capacitance. It is observed that segment A_1 dominates the stored energy, and the contributions of segments B_1 and B_2 are negligible. The design guideline is that increasing the core geometry and increasing distance from segment C to the core will effectively reduce the interwinding capacitance.

C. Measurement Results

Fig. 10 shows the experimental data of the interwinding impedance magnitude and phase of the transformer. It is done with both terminals of each winding shorted. As can be seen, the impedance magnitude has a constant slope with -20 dB/dec roll off, and the phase is around $-90°$. Therefore, the interwinding impedance is capacitive, and it is appropriate to model the interwinding impedance as a lump-element circuit with an interwinding capacitor. The measured data are in the form of digital values of impedance magnitude and phase at a sweep of different frequencies. They are imported into MATLAB and

TABLE II
PARAMETERS OF MAGNETIC CORE AND WINDING GEOMETRIES OF THE TRANSFORMER

Core material	N87
Core dimension	36 mm × 23 mm × 15 mm
Turns ratio	55:11
Primary winding	Litz-wire 60 × 0.2 mm
Secondary winding	copper 1.0 mm
ϵ_0	$8.85.10^{-12}$ F/m
d	1 mm
l	16 mm
r_i	11.5 mm
r_o	18 mm
n_p	55
n_s	11
V_P	300 V
V_S	60 V
r_B	12 mm
l_B	6.5 mm
l_C	16 mm

TABLE III
CALCULATED ENERGY AND CAPACITANCE

Parameter	E_i (J)	E_o (J)	E_B (J)	$E_{C\text{in}}$ (J)	$E_{C\text{out}}$ (J)	E_{total} (J)	C_{int} (F)
Value	1.3 e-7	8.4 e-8	1.1 e-9	3.8 e-8	3.2 e-8	2.9 e-7	9.97 e-12

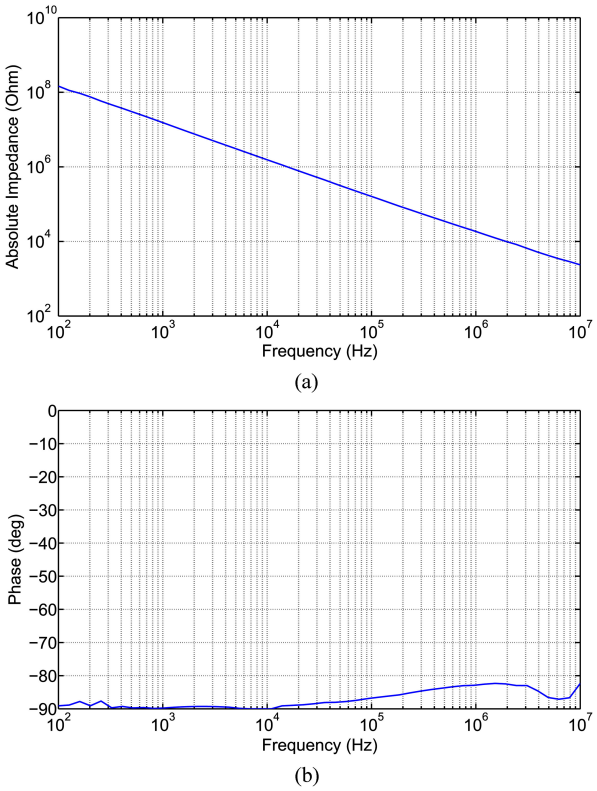

Fig. 10. Interwinding impedance measurement: (a) magnitude and (b) phase.

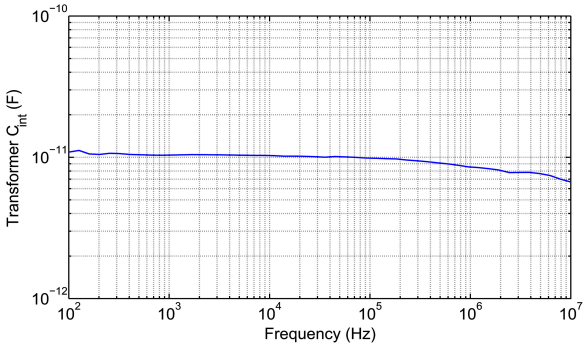

Fig. 11. Measured interwinding parasitic capacitance.

processed by proper scripts to yield the interpreted coupling capacitance, whose values are shown in Fig. 11. It can be seen that the capacitance value is around 10 pF in the wide range of frequency from dc to 10 MHz. It is validated that with the proposed configuration of the transformer, an extremely low interwinding parasitic capacitance can be achieved.

The process is repeated for the measurement of the impedance between two terminals of the primary side while the two terminals of the secondary side shorted. This impedance can be modeled as a leakage inductor. The impedance magnitude and phase are shown in Fig. 12(a) and (b). The impedance behaves like a resistor at frequencies up to 1 kHz due to winding ohmic resistance, like a leakage inductor from 2 kHz to 1.5 MHz due to leakage flux, and like a capacitor from above 1.5 MHz due to the self-capacitance of the leakage inductor. The interpreted magnitude of the leakage inductor is shown in Fig. 12(c). The leakage inductance value is 170 μH in the range of 100–300 kHz. The consequential relatively high leakage inductance may be explained by the large geometrical separation of the two windings that produces relatively large leakage flux outside the core. Hence, the proposed topology as well as its associated control approach must be designed to utilize the leakage inductor. The control approach will be presented in the next section.

VI. PROPOSED CONTROL APPROACH

A. Proposed Control Approach

In this paper, the control approach without isolated feedback is adopted in order to achieve minimum circuit input-to-output parasitic capacitance for the requirements of the targeted applications. The proposed converter physical configuration is shown in Fig. 13. There are two control loops where one resides in the primary and the other one resides in the secondary. The secondary-side controller regulates the output voltage to be constant at 60 V. The primary-side controller controls the primary-side inductor current; thus, it indirectly regulates the nominal output current. The secondary-side circuit can be seen as a current source supplying the output capacitor in parallel with the load.

On the secondary side, the output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch the shunt switch S_5 ON and OFF. When S_5 is switched OFF, the converter operates in its *power mode* [see Fig. 14(a)] and the output

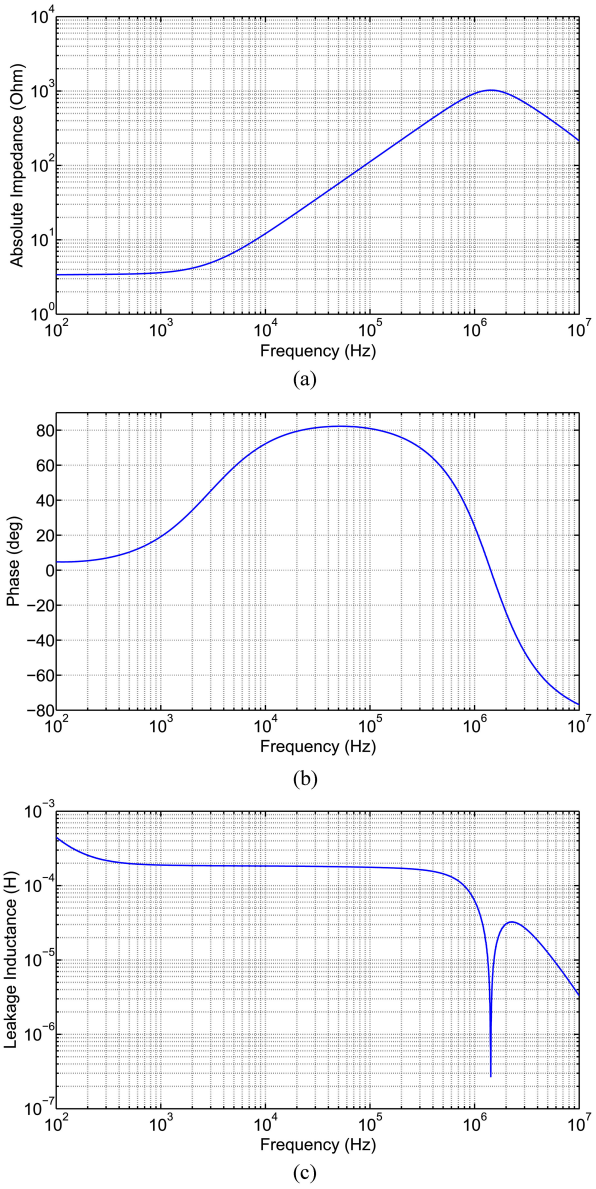

Fig. 12. Primary leakage impedance measurement. (a) Magnitude, (b) phase, and (c) leakage inductance.

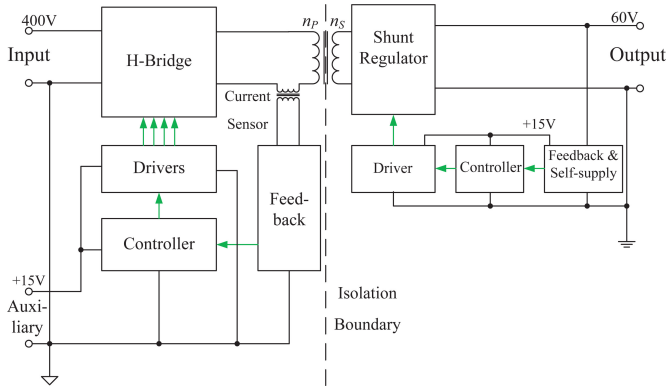

Fig. 13. Block diagram of the circuit layout.

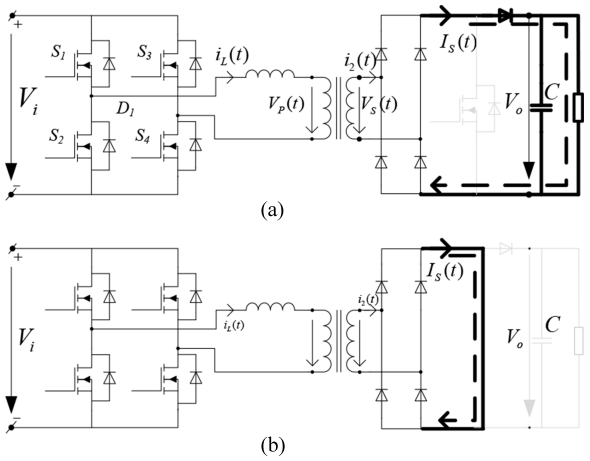

Fig. 14. Operation mode: (a) Power mode and (b) shunt mode.

voltage increases. On the other hand, when S_5 is ON, shunting the secondary side, the converter operates in its *shunt mode*, which is shown in Fig. 14(b); the output voltage decreases. This control approach is different from the control method of the conventional full-bridge topology or single active bridge topology in that the output voltage regulation is independent from the regulation of the active switches of the primary side. Normally, the former topologies involve a feedback of the output voltage across the isolation boundary, and utilization of a compensator to adjust the switching fashion of the active bridge in order to control the output voltage. However, as mentioned in Section III, those topologies and their control approach are not optimal for the targeted applications.

On the primary side, because the leakage inductance is relatively high, at 170 μH, it is utilized as the main inductor in the circuit, and there is no external inductor added. In this way, the leakage inductor, although being relatively high Henry value compared to a traditional converter, has become an integral part of the converter. The primary-side inductor current can be controlled by adjusting one variable among the three variables of the primary switches: frequency, phase shift, and duty cycle. In this paper, the frequency modulation is chosen. The duty cycle of the switches is fixed at 50%, and the phase-shift is therefore at 0°. The primary-side current i_L is first sensed and rectified. It is then low-pass filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analogue proportional-integral (PI) compensator. The output of the PI compensator is fed to a voltage-controlled oscillator (VCO) that automatically adjusts the switching frequency to keep the rectified primary dc current to be a constant 1 A dc. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc. The analytical waveforms of the converter in the two operation modes are shown in Fig. 15, whereas the block diagrams of the two control loops are shown in Fig. 16.

B. Power Mode Operation

The power mode is the operation mode where the shunt MOSFET S_5 is open, allowing the output current to supply the output

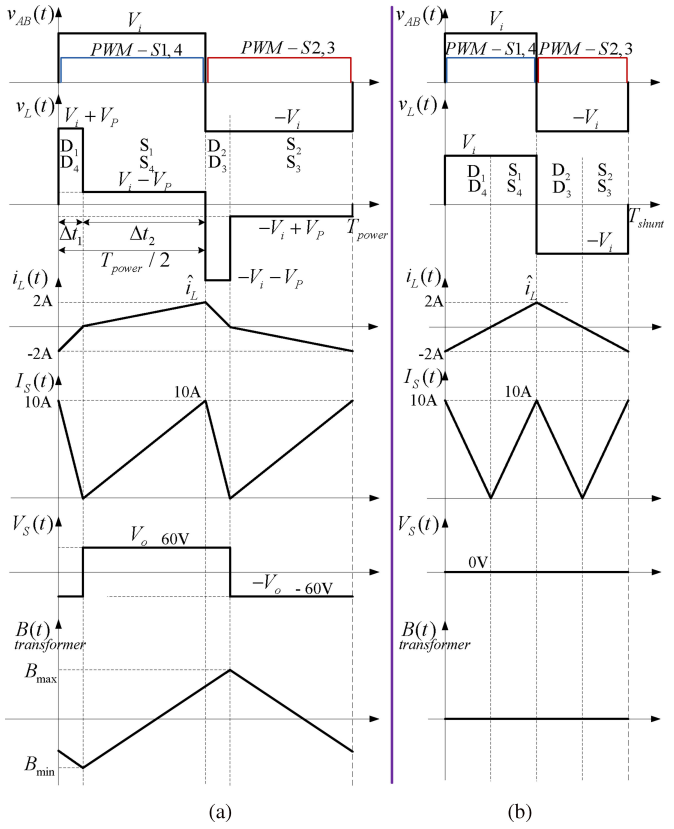

Fig. 15. Analytical waveforms when the converter operates in: (a) Power mode and (b) shunt mode.

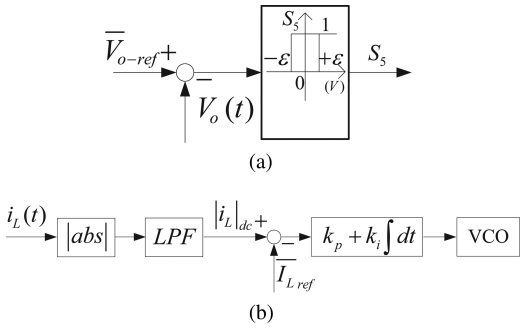

Fig. 16. Control block diagram. (a) Hysteresis control in the secondary side and (b) average current mode control in the primary side.

load as in Fig. 14(a). The analytical waveforms of the converter operating in power mode are shown in Fig. 15(a). As mentioned earlier, the pulse width modulation (PWM) signal for each pair of switches (S_1, S_4) and (S_2, S_3) is a pulse with 50% duty cycle. A complete period consists of 50% of the time where (S_1, S_4) are commanded to turn ON, and 50% of the time where (S_2, S_3) are commanded to turn ON. There is no phase shift between the PWM signals except for a small amount of dead time.

When the PWM signal sent to (S_1, S_4) is ON and the PWM signal sent to (S_2, S_3) is OFF, the inductor current $i_L(t)$ will increase from the most negative value $-\widehat{i}_L$ to the most positive value $\widehat{i}_L$. During the duration where $i_L(t)$ is increasing from $-\widehat{i}_L$ to zero, the body diodes (D_1, D_4) of the two switches conduct the current [see Figs. 1 and 15(a)]. Because $i_L(t)$ is negative during this duration, the secondary-side current $i_2(t)$ is negative; it conducts through diodes (D_{S2}, D_{S3}). The voltage across the secondary winding is $V_S(t) = -V_o$, which is a negative value. This voltage is reflected to the primary side by the turns ratio: $V_P(t) = (n_P/n_S)V_S(t) = -(n_P/n_S)V_o = -V_P$, where $V_P(t) = V_P \text{sgn}(i_L(t))$ and the operator sgn denotes the sign of the operand.

As a result, the voltage across the leakage inductor during the time when the inductor current is negative is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = V_i + V_P$. The current increases linearly with time with a slope of $(V_i + V_P)/L$.

After the inductor current reaches zero, diodes (D_1, D_4) stop conducting and the current flows through the channels of (S_1, S_4) instead. This results in a zero voltage, zero current switching at turn-on of switch (S_1, S_4). This means there is no switching loss in turning ON switches (S_1, S_4), and it is one of the advantages of this control approach. The inductor current changes direction to positive, as does the secondary-side current $i_2(t)$. Current $i_2(t)$ flows through diodes (D_{S1}, D_{S4}), making the voltage across the secondary-side transformer positive, $V_S(t) = V_o$. Hence, the voltage across the primary side of the transformer becomes positive.

The voltage across the leakage inductor during the time when the inductor current is positive is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = V_i - V_P$. The slope of the current during this duration is $(V_i - V_P)/L$ [see Fig. 15(a)].

During the next half-period, the PWM signal of switches (S_1, S_4) is OFF and the PWM signal of switches (S_2, S_3) is ON. At the transition of these PWM signals, (S_1, S_4) is turned OFF and, because the current is positive, it is transferred from the channels of (S_1, S_4) to the body diodes (D_2, D_3) of switches (S_2, S_3). The voltage difference between two nodes A and B changes polarity. The voltage across the inductor is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = -V_i - V_P$ as long as the inductor current is positive. When the inductor current decreases and reaches zero, the body diodes (D_2, D_3) stop conducting and the current is transferred to the channels of switches (S_2, S_3). Again, the turn-on transient of switches (S_2, S_3) occurs with the zero voltage, zero current feature, resulting in no switching loss. Similarly, when the inductor current is negative and (S_2, S_3) are ON, the voltage across the inductor is $-V_i + V_P$.

Based on the above analysis, the inductor current has the resulting form which is shown in Fig. 15(a). It is a nonsymmetrical triangular ac signal with zero dc bias. Due to the presence of the diode bridge in the secondary side, the output current $I_S(t)$ is the result of the rectified inductor current multiplying with the inversion of the turns ratio

$$I_S(t) = |i_2(t)| = \frac{n_p}{n_s}|i_L(t)|. \tag{16}$$

Diode D_{S5} in the power mode is forward-biased. The output current $I_S(t)$ is a positive triangular signal with twice the frequency of the leakage inductor current. Its peak value is $(n_P/n_S)\widehat{i}_L$ or 10 A in this design. The dc value of this signal is therefore half its peak value: $0.5(n_P/n_S)\widehat{i}_L$ or 5 A.

The switching frequency that ensures the primary side is regulated at the peak value of $\widehat{i}_L$ can be derived by equating the product of voltage across the inductor and time when the current is negative to that when the current is positive. The peak value when the inductor current is negative is equal to that when the current is positive (see Fig. 15)

$$\widehat{i}_L = \frac{V_i + V_P}{L}\Delta t_1 = \frac{V_i - V_P}{L}\Delta t_2, \tag{17}$$

where

$$\Delta t_1 + \Delta t_2 = \frac{T}{2} = \frac{1}{2f}. \tag{18}$$

From (17) and (18), it can be proved that

$$f = \frac{V_i}{4\widehat{i}_L L}\left(1 - \left(\frac{V_P}{V_i}\right)^2\right). \tag{19}$$

As a result, the switching frequency in power mode is

$$f_{\text{power}} = \frac{V_i}{4\widehat{i}_L L}\left(1 - \left(\frac{n_p V_o}{n_s V_i}\right)^2\right). \tag{20}$$

Given the input and output voltage value from Table I, leakage inductor $L = 170\ \mu$H, peak value of the inductor current $\widehat{i}_L = 2$ A, we can derive the expected switching frequency in power mode: $f_{\text{power}} = 128$ kHz.

C. Shunt Mode Operation

The shunt mode is the operation mode where the shunt MOSFET S_5 is shorted, which is illustrated in Fig. 14(b). The voltage of the anode of diode D_{S5} with respect to the secondary-side return path is approximately zero if the voltage across the on-resistance of S_5 is neglected. Because the output voltage is regulated at V_o and there is an output capacitor C that prevents output voltage from being changed drastically, the voltage at cathode of D_{S5} is V_o. Hence, D_{S5} is reverse-biased.

In a similar way, the analytical waveforms of the converter operating in shunt mode are shown in Fig. 15(b). Because now the shunt switch is shorted, the output current $I_S(t)$ will circulate through either (D_{S1}, S_5, D_{S4}) or (D_{S2}, S_5, D_{S3}) when the secondary-side current $i_2(t)$ is positive or negative, respectively. The voltage across the secondary-side transformer, $V_S(t)$, becomes zero, which is demonstrated in the bottom of Fig. 15(b). Thus, $V_P(t)$ also becomes zero.

As a result, the voltage across the leakage inductor when the PWM signal for (S_1, S_4) is ON is V_i regardless of the sign of the current. Likewise, the voltage across the leakage inductor when the PWM signal for (S_2, S_3) is ON is $-V_i$. This results in a symmetrical leakage inductor current as shown in Fig. 15(b). The output current $I_S(t)$ is a symmetrical positive signal.

From (19), given $V_P = 0$, the expected switching frequency in shunt mode is

$$f_{\text{shunt}} = \frac{V_i}{4\widehat{i}_L L}. \tag{21}$$

The calculated expected switching frequency in shunt mode is, therefore, $f_{\text{shunt}} = 294$ kHz.

D. Comparison With Existing Control Approaches

A very loosely coupled transformer, as is the case here, has a significant high leakage inductance. This is, in this paper, used as the inductance of the circuit (see Fig. 1). Many resonant converters utilize similar concept [24]–[26]. The practice of using the high leakage inductance as the main inductor is also adopted in dual active bridge converters [34]–[36]. In this paper, the control circuit, to some extent, can be regarded as nonconventional. The primary side uses a combination of average current mode (peak current mode could also be used) and variable frequency control to keep the inductor current at a constant level. However, average and peak current mode controls are conventional control methods [37]–[40]. Variable frequency control is widely used by many resonant converters [24]–[26], [41]. In this paper, those two methods are combined on the primary side. On the secondary side, the output voltage hysteresis control of the shunt switch is used. This practice, to some extent, can be regarded as nonconventional, but relatively straight forward to implement.

Using the combination of the previously mentioned primary- and secondary-side controls enables a complete elimination of the feedback loop crossing the isolation boundary, which would, in almost all implementations, imply additional parasitic capacitance added (such as the input–output capacitance of an optocoupler or of a high-frequency feedback transformer) between primary and secondary sides.

VII. Experimental Results

The specifications of the converter were described in Section II, and they will be summarized briefly here. The input voltage to the converter is 400 V dc, which represents the output of a typical power factor correction circuit. The inductor current is to be controlled at 2 A peak. This results in a rectified current of 10 A peak in the output because the turns ratio of 5:1 is used. The dc offset value of the secondary-side rectified current $I_S(t)$ is therefore 5 A. The output voltage is controlled at 60 V. This allows the converter to output 300-W nominal power. The expected switching frequency of the active bridge in steady state in shunt and power modes is 294 and 128 kHz, respectively. Most importantly, an overall circuit input-to-output capacitance of no more than 10 pF is desired.

The experimental studies have examined circuit input-to-output parasitic capacitance, converter transient response, and converter power efficiency. A photo of the prototype can be found in Fig. 17. As can be seen from the photo, the proposed transformer is the only element that links between the primary side and secondary side. There is no feedback element added across the isolation boundary.

A. Circuit Input-to-Output Parasitic Capacitance

The circuit input-to-output capacitance is measured by the Agilent 4294A precision impedance analyzer. The accuracy claimed by the manufacturer is $\pm 3\%$ in the measured range. The two input terminals are shorted and so are the two output terminals. After that, the ground planes of the primary side and secondary side are measured with the instrument. Fig. 18 shows

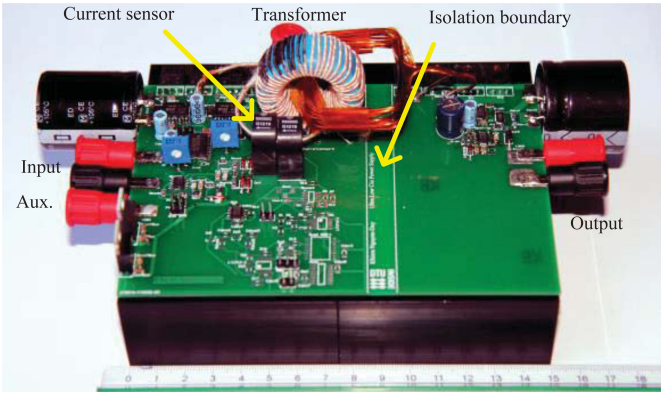

Fig. 17. Photo of the prototype.

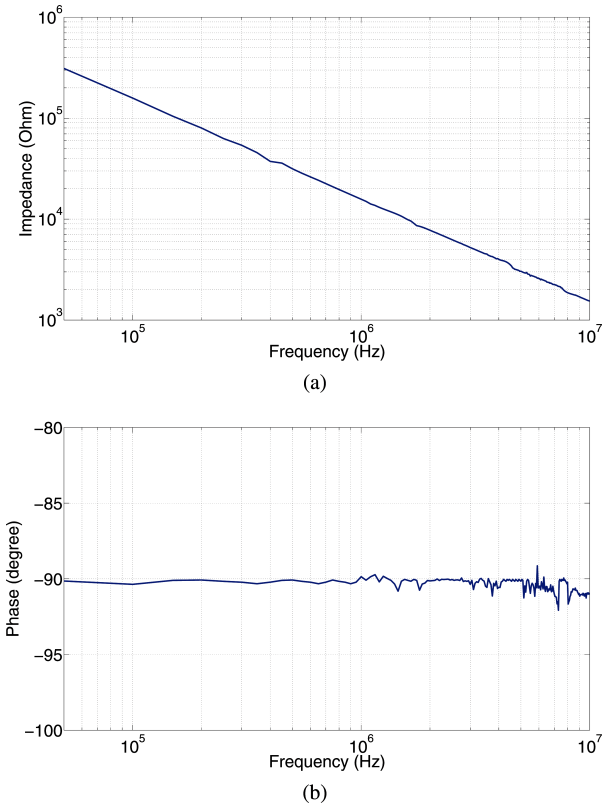

Fig. 18. Circuit input-to-output impedance measurement: (a) magnitude and (b) phase.

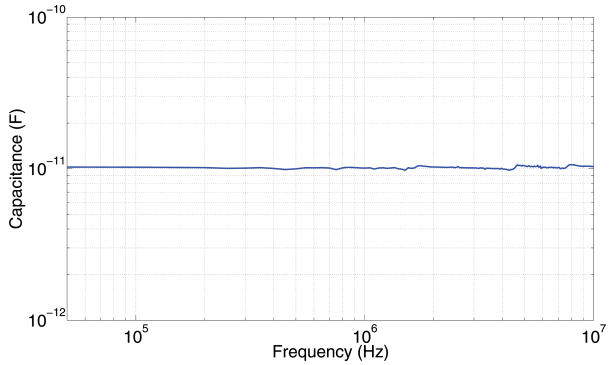

Fig. 19. Circuit input-to-output parasitic capacitance.

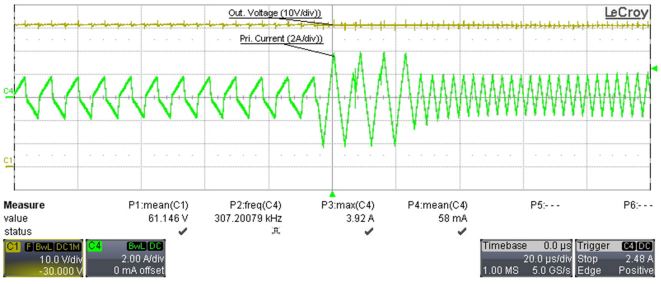

Fig. 20. Transient response from power mode to shunt mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

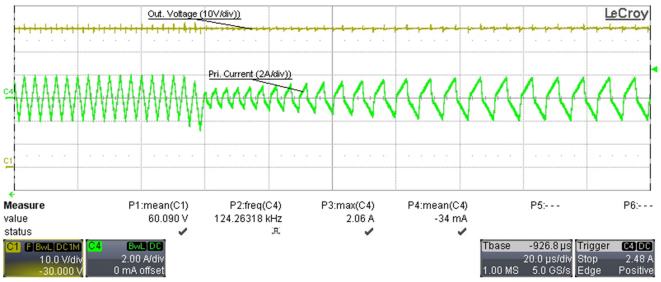

Fig. 21. Transient response from shunt mode to power mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

the circuit input-to-output impedance magnitude and phase measurement. Its magnitude slope of -20 dB/dec and phase around -90° makes it appropriate to model as a capacitor. The measured value of the capacitance is around 10 pF, which is shown in Fig. 19. In short, an extremely low value of circuit input-to-output capacitance has been achieved, and it has been proven to be dominated by the interwinding parasitic capacitance.

B. Converter Transient Response

In this section, two key measurement waveforms are presented and discussed. They are the inductor current on the primary side and the output voltage on the secondary side. The measurement of the inductor current is performed by the LeCroy AP015 current probe, which has a claimed accuracy of $\pm 1\%$. In addition, the measurement of the output voltage is done with the SI-9000 differential probe with an accuracy of $\pm 2\%$ as claimed by the manufacturer.

Fig. 20 shows the transient response from power mode to shunt mode. In a similar way, the transient from shunt mode to power mode is shown in Fig. 21. The value of the output voltage threshold, ε, is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady-state values, which are 2 A peak and 60 V dc, respectively. The transient of the current from power mode to shunt mode and vice versa finishes within about 30 and 40 μs, respectively. The time needed for the inductor current

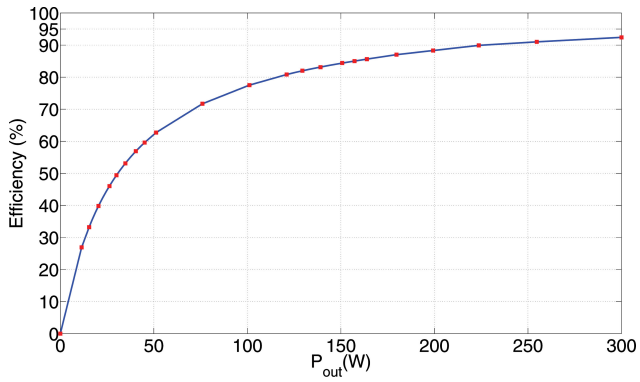

Fig. 22. Converter's power efficiency.

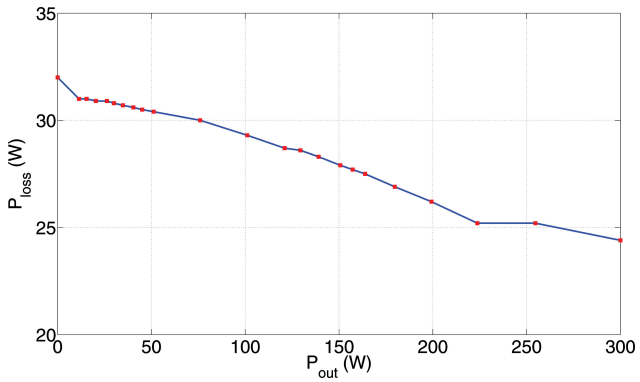

Fig. 23. Converter's power loss.

to settle is mainly determined by the dynamic of the average current control scheme described in Fig. 16. The experimental switching frequencies of the primary-side switches in power mode and shunt mode are 124 and 307 kHz, respectively. They are respectively 3% and 4% different from the expected values derived in Section VI. This is simply due to the tolerance of the components used in the analogue control circuitry and sensing, and the ignorance of the small forward voltage drop in the diodes on the secondary side. Nevertheless, the transient and steady state are both stable and satisfactory. The behavior of the circuit matches accurately with the aforementioned circuit analysis.

C. Converter Power Efficiency

The power measurement is done with the PPA5530 precision power analyzer. The accuracy claimed by the manufacturer is $\pm 0.4\%$ in the operation condition under test. The measured efficiencies at different output powers are shown in Fig. 22. At the nominal output of 300 W, the converter operates entirely in its power mode. The switching frequency on the primary side is then the smaller one, f_{power}. Therefore, the primary switching loss and both conduction loss and switching loss of shunt MOSFET S_5 are reduced. That is the reason why the peak efficiency is attained at the nominal output power. This value is 92.4%. As output power reduces, the duration in which the converter operates in shunt mode increases linearly; the loss increases slightly as shown in Fig. 23. As a result, the efficiency drops. Zero efficiency is attained at zero output power when the converter fully operates in its shunt mode. In general, the overall efficiency of the converter is satisfactory particularly ranging from 1/3 nominal power to full nominal power. Its efficiency in this range is from 77.5% to 92.4%.

VIII. Discussion

This study has been primarily concerned with minimizing converter input-to-output parasitic capacitance in order to achieve maximum noise immunity to high *dv/dt* from the loads. This goal has been approached by fulfilling two objectives. First, a novel topology with minimized interwinding capacitance transformer has been introduced. Second, a new control strategy has been proposed that both eliminates the feedback path across the isolation boundary and maintains the desired output voltage.

If a conventional full-bridge converter is used, taking the isolated boost converter as an example, the transformer should then be required to have a very low leakage inductance. Such a transformer will require very close proximity between the windings. Because the interwinding capacitance is inversely proportional to the relative distance between the windings, this configuration therefore increases the transformer parasitic capacitance. Additional EMI filtering, if added to the full-bridge converter, would not correct the high input-to-output capacitance. While the added secondary switch increases size and cost, the major goal is high *dv/dt* immunity between the primary and secondary, which provides good CM immunity.

Several advantages of the developed converter's prototype and its control strategy are as follows. First, the topology and its control allow zero current, zero voltage switching at the turn-on transitions of the switches (refer to Fig. 15 and the discussion in Section VI-B), resulting in lower switching loss at turn-on transients.

Second, this topology has higher power (60 V/300 W) per channel than 36 V/5 W designs of prior art [1] with a similar topology. This allows the converter to supply a wider range of load, from 0 to 60 V and up to 300 W.

Third, the proposed control strategy improves the reliability of the control electronics because there are no feedback elements across the isolation boundary. Specifically, it provides a more reliable fault protection if necessary because input and output voltage or current levels can be monitored and fault protection can be triggered with minimum delay.

Fourth, the regulation of the output power is very fast. Whenever the output current is not consumed by the load, it is circulated through the shunt-switch and the secondary-side diode bridge. As soon as S_5 is turned OFF, there will be 300 W of power immediately available to supply the output. Furthermore, the elimination of feedback prevents saturation of the control circuitry during transients. All of these proposed topology and control features make the converter react very quickly to changes in power demand compared to existing topologies and controls.

Finally, an extremely low circuit input-to-output capacitance is achieved: 10 pF in a 300-W prototype. Its parasitic

capacitance per watt is 0.033 pf/W, which is approximately 30 times lower than that of existing converters reported in the literature [12], [13].

It must be acknowledged, however, that the proposed approach contains several disadvantages. First, the MOSFETs on the primary side turn off at their peak currents, resulting in higher turn-off loss. Second, the slightly increased loss at lighter load makes the converter's efficiency relatively low at low output power. This issue may be considered in a separate study.

IX. Conclusion

In this paper, the authors have presented the design of a 300-W isolated power supply with very high *dv/dt* immunity. The main advantage of the power supply is the extremely low interwinding capacitance in the transformer, which makes the circuit input-to-output capacitance ultralow, considering the output power. The converter is specially designed for applications with very large changes of voltage over short durations of time. Circuit operation and control have been presented, and experimental data have also been provided that prove to match well with expectations. Furthermore, the advantages and disadvantages of the converter have been discussed. In summary, the converter is suitable for a wide range of applications, especially where fast output power response and minimization of the circuit input-to-output capacitance are vital.

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References

[1] M. A. E. Andersen, "MOS gate driver circuit with extremely high galvanic isolation," in *Proc. Eur. Conf. Power Eletron. Appl.*, 1995, pp. 747–551.

[2] D. Knurek, "Reducing EMI in switch mode power supplies," in *Proc. 10th Int. Telecommun. Energy Conf..*, 1988, pp. 411–420.

[3] (Mar. 2011). Auxilliary power supplies for medium and high voltage applications. in *Proc. Bodo's Power Syst.* [Online]. Available: http://www.gva-leistungselektronik.de/_gva/gva_downloads/GvA_Auxiliary_Power_Supplies.pdf

[4] S. Wang, P. Kong, and F. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[5] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1095–1099, Dec. 2003.

[6] D. Fu, S. Wang, P. Kong, F. Lee, and D. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[7] M. Borage, S. Tiwari, and S. Kotaiah, "Common-mode noise source and its passive cancellation in full-bridge resonant converter," in *Proc. 8th Int. Conf. Electromagn. Interference Compat.*, 2003, pp. 9–14.

[8] P. Kong, S. Wang, F. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.

[9] W. Hong and R. O'Connell, "Effects of parasitic transformer capacitances on switching transients at a HV capacitor bank," in *Proc. 40th North Amer. Power Symp.*, 2008, pp. 1–6.

[10] W. Xin, F. N. K. Poon, C. M. Lee, M. Pong, and Z. Qian, "A study of common mode noise in switching power supply from a current balancing viewpoint," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, vol. 2, pp. 621–625.

[11] J.-h. Choi, M. Madafshar, and K. Parmenter, "Designing common-mode (CM) EMI noise cancellation without y-capacitor," in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf.*, 2007, pp. 936–940.

[12] D. Garabandic, W. Dunford, and M. Edmunds, "Zero-voltage-zero-current switching in high-output-voltage full-bridge PWM converters using the interwinding capacitance," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 343–349, Mar.1999.

[13] P. Kong and F. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo*, 2010, pp. 1424–1429.

[14] "Interlink coupling high-voltage impact isolation transformer," cN Patent 2318 700, May 12, 1999. [Online]. Available: https://www.google.com/patents/CN2318700Y?cl=en

[15] (Dec. 4, 2012). Medium-voltage high-speed switches with IGBT power semiconductors. *Bodo's Power Syst*. [Online]. Available: http://www.powerguru.org/medium-voltage-high-speed-switches-with-igbt-power-semiconductors

[16] M. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, Sep. 2008.

[17] M. Hoyerby, and M. A. E. Andersen, "Optimized envelope tracking power supply for tetra2 base station RF power amplifier," in *Proc. 23th IEEE Annu. Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 777–783.

[18] M. Hoyerby and M. A. E. Andersen, "TEDS base-station power amplifier using low-noise envelope tracking power supply," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1687–1693, Jul. 2009.

[19] (2013, Feb. 25). Power electronics for medium-voltage applications, *Bodo's Power Syst.* [Online]. Available: http://www.powerguru.org/power-electronics-for-medium-voltage-applications/

[20] "An-1095 design of isolated converters using simple switchers," (2013, Apr.) Appl. Note. [Online]. Available: http://www.ti.com/lit/an/snva005b/snva005b.pdf

[21] (2013, Oct.). Miniature surface mount transformer, Document 606-1. [Online]. Available: http://www.coilcraft.com/mintrans.cfm

[22] (2014). Max250/max251 compatible converter transformers. 78250 Series. [Online]. Available: http://www.murata-ps.com/data/magnetics/kmp_78250.pdf

[23] A. J. Binnie and T. R. Foord, "Leakage inductance and interwinding capacitance in toroidal ratio transformers," *IEEE Trans. Instrum. Meas.*, vol. 16-IM, no. 4, pp. 307–314, Dec.1967.

[24] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.

[25] W. Feng, F. Lee, and P. Mattavelli, "Optimal trajectory control of LLC resonant converters for led PWM dimming," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 2, pp. 979–987, Feb. 2014.

[26] W. Feng and F. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.

[27] K. Nguyen-Duy, L. Petersen, A. Knott, O. Thomsen, and M. A. E. Andersen, "Design of a 300-Watt isolated power supply with minimized circuit input-to-output parasitic capacitance," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drive*, Apr. 8–10, 2014, pp. 1–6.

[28] Z. Ouyang, O. Thomsen, and M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.

[29] J. Biela and J. Kolar, "Using transformer parasitics for resonant converter—A review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[30] L. Dalessandro, F. da Silveira Cavalcante, and J. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[31] H.-Y. Lu, J. G. Zhu, and S. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.

[32] T. Duerbaum and G. Sauerlaender, "Energy based capacitance model for magnetic devices," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, vol. 1, pp. 109–115.
[33] K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, "Minimization of the transformer interwinding parasitic capacitance for modular stacking power supply applications," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 26–28, Aug. 2014.
[34] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 8, pp. 3931–3940, Aug. 2013.
[35] H. van Hoek, M. Neubert, and R. De Doncker, "Enhanced modulation strategy for a three-phase dual active bridge–boosting efficiency of an electric vehicle converter," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 12, pp. 5499–5507, Dec. 2013.
[36] G. Oggier, M. Ordonez, J. Galvez, and F. Luchino, "Fast transient boundary control and steady-state operation of the dual active bridge converter using the natural switching surface," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 946–957, Feb. 2014.
[37] J.-W. Shin and B.-H. Cho, "Digitally implemented average current-mode control in discontinuous conduction mode PFC rectifier," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3363–3373, Jul. 2012.
[38] Y. Yan, F. Lee, and P. Mattavelli, "Analysis and design of average current mode control using a describing-function-based equivalent circuit model," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4732–4741, Oct. 2013.
[39] J. Wang and J. Xu, "Peak current mode bifrequency control technique for switching dc–dc converters in DCM with fast transient response and low EMI," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1876–1884, Apr. 2012.
[40] M. Hallworth and S. Shirsavar, "Microcontroller-based peak current mode control using digital slope compensation," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3340–3351, Jul. 2012.
[41] Q. Zhang, C. Hu, L. Chen, A. Amirahmadi, N. Kutkut, Z. Shen, and I. Batarseh, "A center point iteration MPPT method with application on the frequency-modulated LLC microinverter," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1262–1274, Mar. 2014.

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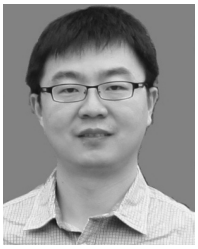

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A.4 (EPE2014)-Minimization of the Transformer Inter-winding Parasitic Capacitance for Modular Stacking Power Supply Applications

Paper A.4. is entitled "Minimization of the Transformer Inter-winding Parasitic Capacitance for Modular Stacking Power Supply Applications." Presented in The 16th European Conference on Power Electronics and Applications (EPE'14), Lappeeranta, Finland, 26-28 August 2014.

Minimization of the transformer inter-winding parasitic capacitance for modular stacking power supply applications

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Keywords

«Parasitic capacitance», «current transformers», «dc-dc power converters», «electromagnetic devices»

Abstract

In an isolated power supply, the inter-winding parasitic capacitance plays a vital role in the mitigation of common mode noise currents created by fast voltage transient responses. The lower the transformer inter-winding capacitance, the more immune the power supply is to fast voltage transient responses. This requirement is even more critical for modular stacking applications in which multiple power supplies are stacked. This paper addresses the issue by presenting a detailed analysis and design of an unconventional isolated power supply that uses a ring core transformer with a very low inter-winding parasitic capacitance of 10 pF. Considering its output power of 300 W, this approach yields about 0.033 pF/W inter-winding capacitance over output power, approximately thirty times lower than existing approaches in the literature. This makes the converter a suitable solution for modular stacking of fast voltage switching applications. Mathematical derivation of the inter-winding capacitance and experiments are carried out to prove the validity of the approach.

Introduction

In isolated power supply applications, the transformer parasitic capacitance can have a significant effect to the converter operation [1-2]. Some of the adverse effects are distortion of the current waveform on the excitation side or a decrease in the overall converter efficiency. Subjected to high-voltage stresses, the inter-winding capacitance causes leakage currents and, consequently, EMI problems [3-6]. However, most publications about the transformer design concern the reduction in leakage inductances and high-frequency winding losses, while winding capacitances have rarely been considered effectively. Limiting the inter-winding capacitance is critical for stacking of power supplies because large inter-winding capacitance creates a significant amount of common mode noise at high frequency [6-7]. Existing transformers in a 1.2 kW converter design are reported to have 1.5 nF inter-winding capacitance [8]. An E-core transformer used in fly-back converter with a power rating of 30 W is reported in [9] to have 34 pF of inter-winding capacitance.

One of the primary applications of this work is supplying energy for ultra-fast tracking converters. Fig. 1 shows a configuration in which multiple modules of the proposed power supply provide energy to multiple modules of the ultra-fast tracking converter. The ultra-fast tracking converters are typical of

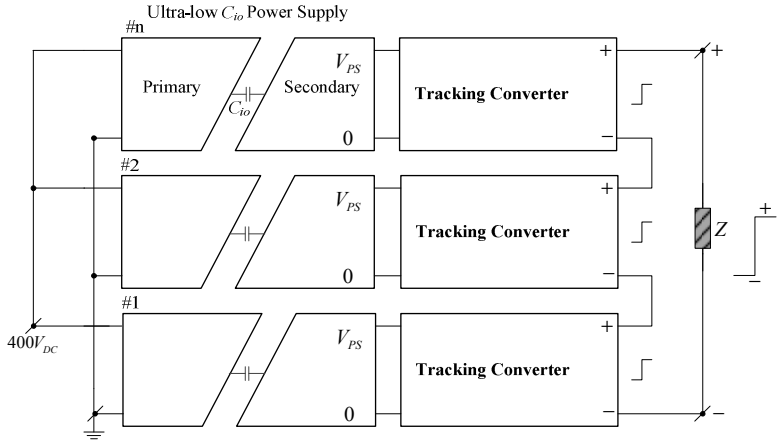


Fig. 1. A typical modular stacking application of power supplies.

radio frequency power amplifiers used in communication system based stations [10]. Due to the high dv/dt at the output of the tracking converters, there will be a large amount of conductive common mode current draw from their output. This current is linearly proportional to the input-output capacitance of the power supply:

$$i_{com} = C_{io}\frac{dV}{dt}. \tag{1}$$

Take, for example, a configuration with three stacked power supply-tracking converters. The tracking converter outputs are connected in series to increase the voltage. The rate of change at the output voltage is 1000 V/μs. Suppose we have a change from 0 to 1000 V in one micro second. The first converter output experiences a change of 333 V/μs. The second converter output experiences a change of 666 V/μs. The third one experiences a change of 1000 V/μs. The coupling current through the circuit input-to-output parasitic capacitance is as follows.

For the first converter:

$$i_{common1} = C_{io}\frac{dV}{dt} = 10pF\frac{333V}{1us} = 3.33mA. \tag{2}$$

For the second converter:

$$i_{common2} = C_{io}\frac{dV}{dt} = 10pF\frac{666V}{1us} = 6.66mA. \tag{3}$$

For the third converter:

$$i_{common3} = C_{io}\frac{dV}{dt} = 10pF\frac{1000V}{1us} = 10mA. \tag{4}$$

These currents are drawn from the tracking converters' output. Therefore, they distort the output current waveforms of the tracking converters, and the performance of the tracking is impaired. The adverse effects become worse when the number of stacked power supplies increases. Therefore, in order to rapidly change the tracking converter output voltage, the circuit input to output parasitic capacitance must be minimized, especially in modular stacking power converter applications. Note also that having minimal circuit input-to-output parasitic capacitance provides an advantage not only for fast changing voltage applications but also for other slower dynamic converters in terms of conducted noise immunity.

This paper studies the converter topology in Fig. 2, which was first presented in [1]. The primary goal is to attain a low transformer inter-winding parasitic capacitance; specifically, 10 pF in a 300 W output power design. Mathematical derivation of the transformer inter-winding capacitance and circuit operation will be presented.

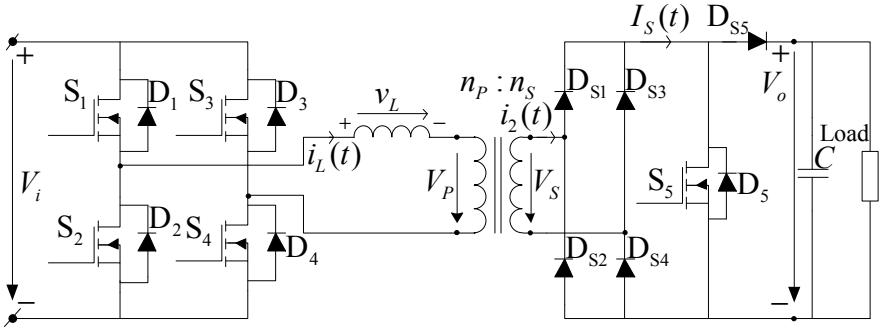


Fig. 2. Topology of the examined converter.

Circuit operation

Suppose that at the input, a power factor correction converter that converts a single phase 220 V ac into 400 V dc is used as the upstream converter. The magnitude of input voltage is therefore 400 V dc. The output voltage is 60 V dc. The output current is designed to be 5 A dc maximum. The maximum output power that is available in the output terminals is 300 W. Higher output voltage or higher output current can be achieved by stacking multiple converters in series or parallel.

The design of a transformer that possesses very low inter-winding capacitance normally involves loose coupling of the transformer windings. This results in the transformer having a relatively high leakage inductance. This high leakage inductance must be utilized with a proper selection of a suitable topology. Examples of suitable topologies are resonant converters [11-12] and the dual active bridge converter [13-14]. The proposed topology in Fig. 2. is, to some extent, similar to a single active bridge [15-16]. However, there are differences in the secondary side configuration and large differences in the control approach compared to those existing topologies. A single active bridge converter does not have the shunt switch as in the proposed converter. All of the control of the output voltage and output current in a single active bridge converter are performed on the primary side. On the contrary, with the utilization of the shunt switch S_5 as in the proposed topology, it is possible to control the output voltage independently on the secondary side; the advantage is the elimination of any necessary control feedback from one side to the other.

Existing control approaches in isolated power supplies usually involve feedback from one side to the other across the isolation boundary [11-16]. These approaches, however, introduce additional parasitic capacitance from the feedback elements, such as high frequency transformers and opto-couplers, which increase the total circuit input-to-output capacitance and degrade the immunity against fast step voltages. For that reason, in this paper, a control approach without isolated feedback is adopted to achieve minimum circuit input-to-output parasitic capacitance and maximum immunity to fast step voltage responses. The block diagram of the proposed circuit layout is shown in Fig. 3.

There are two control loops whose block diagrams are shown in Fig. 4. The secondary side controller regulates the output voltage to be constant at 60 V. The output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch on and off the shunt switch S_5. When the switch S_5 is on, shunting the secondary side, the converter operates in its shunt mode (see Fig.5a,c), and the output voltage decreases. Vice versa, when S_5 is off, the converter operates in its power mode, which is shown in Fig. 5b,c; the output voltage increases. In the primary side control, the primary side current i_L is sensed. It is rectified and filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analog proportional-integrator (PI) controller. The output of the PI controller is fed to a voltage-controlled oscillator (VCO) that will automatically adjust the switching frequency to keep the rectified primary dc current to be constant at 1 A dc. The duty cycle of the primary switches is regulated at 50 %. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc.

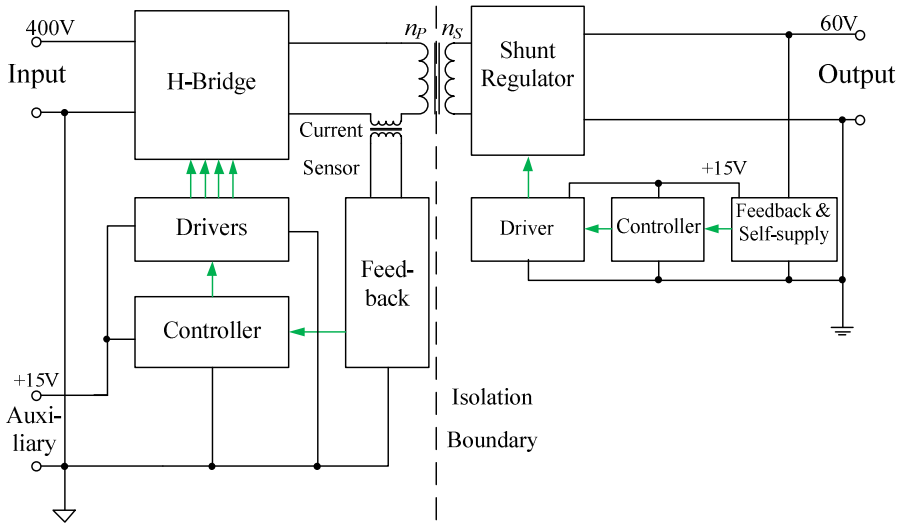


Fig. 3. Block diagram of the circuit layout.

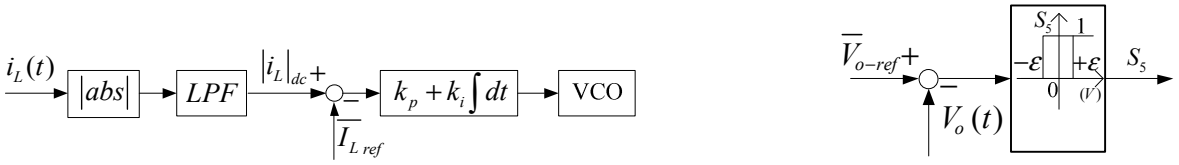


Fig. 4. Control block diagram: a) average current mode control in the primary side b) hysteresis control in the secondary side.

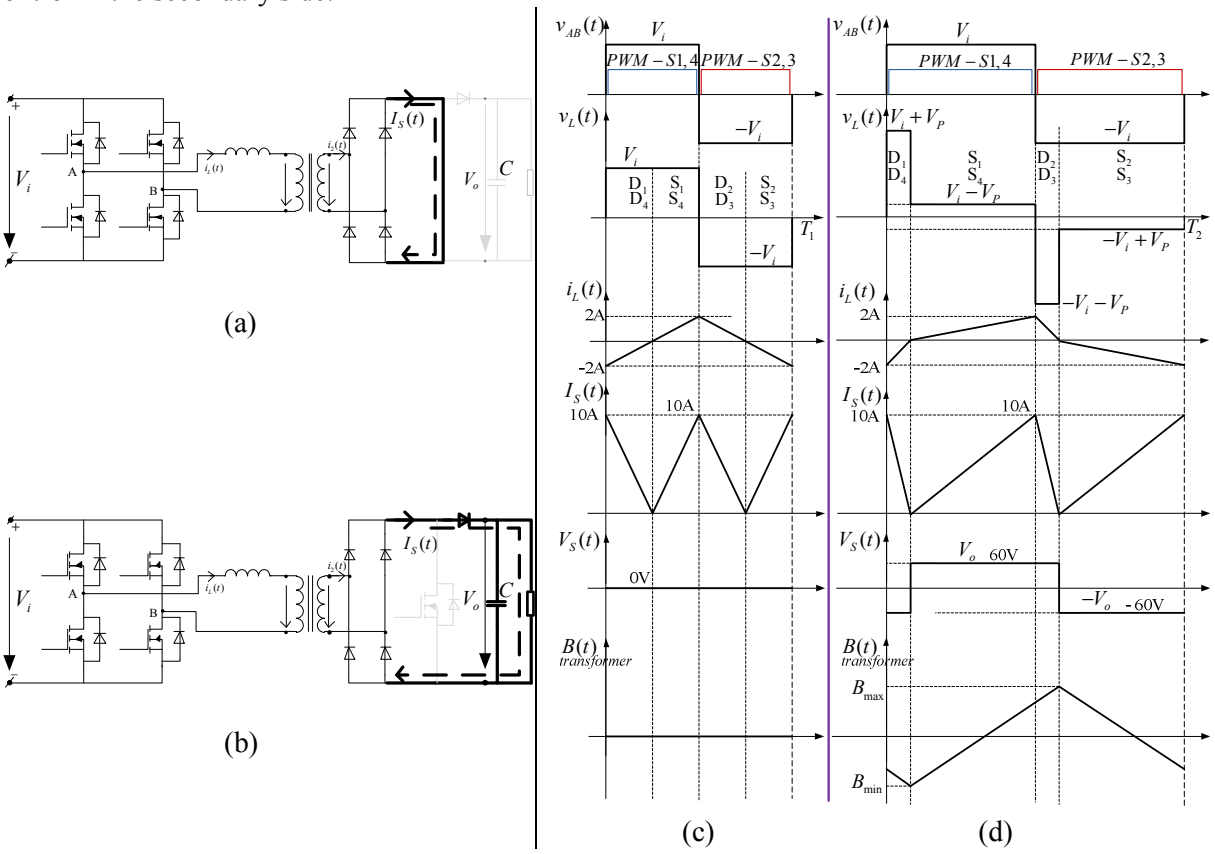
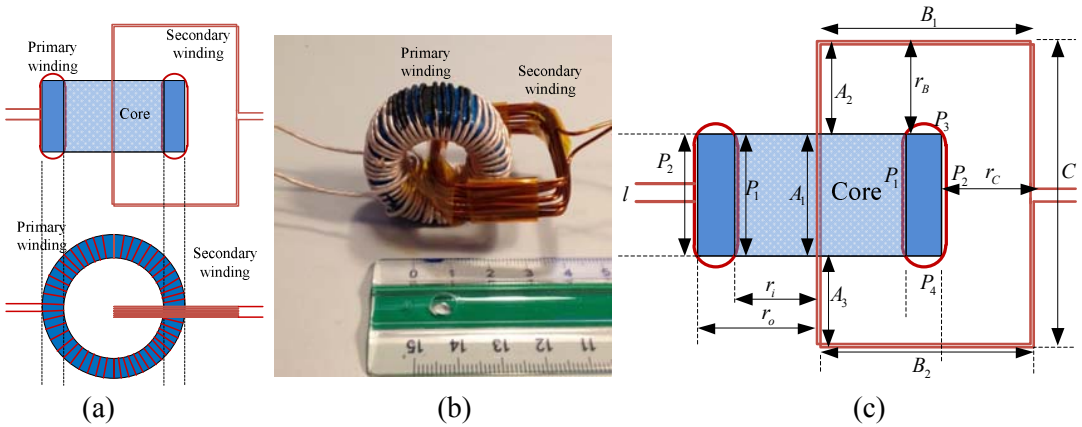


Fig. 5. Operation modes a) shunt mode, b) power mode. Analytical waveforms when converter operates in c) shunt mode, and d) power mode.

Calculation of the transformer inter-winding capacitance

The general structure of the transformer under test is illustrated in Fig. 6a, and the transformer prototype photo is in Fig. 6b. In its winding configuration, the winding with fewer turns will be placed in the geometrical center of the core. It forms a rectangular frame symmetrically around the core. The remaining winding, with more turns is wounded tightly around the core. This is respectively the case of the secondary winding and primary winding in Fig. 6b.



(a) (b) (c)

Fig. 6. Transformer structure: a) conceptual structure b) the transformer under test. c) winding geometry convention

It should be noted that, in general, ferrite does not cause a significant change in the parasitic capacitance. But ferrite with high conductivity material and very high operation frequency may cause a change on the parasitic capacitance. In this work, material N87 [17] is used for the ferrite core and is not considered to have high conductivity. Therefore, its effect on the parasitic capacitance can be ignored.

The inter-winding capacitance can be calculated by using the stored electric energy method, in which voltage distribution plays a vital role.

First, the inter-winding capacitance caused by the interaction between segment A_1 of the secondary winding through the core center to the parallel segments P_1 and P_2 of the primary winding (see Fig. 6c) will be calculated. Segments P_1 and P_2 are the winding parts around the perimeters of the inner ring and outer ring, respectively. Table I provides dimensional information of the core and winding with respect to the notations in Fig. 6c. The secondary has 11 turns stranded together, so each turn can be approximately treated as located in the center of the magnetic core, as shown in Fig. 7. The static capacitance between the inner primary turns and the secondary turns can be expressed as [4, 6]:

$$C_i = \frac{\varepsilon_0 S}{r_i} = \frac{\varepsilon_0 d\pi l}{2 \cdot r_i}, \tag{5}$$

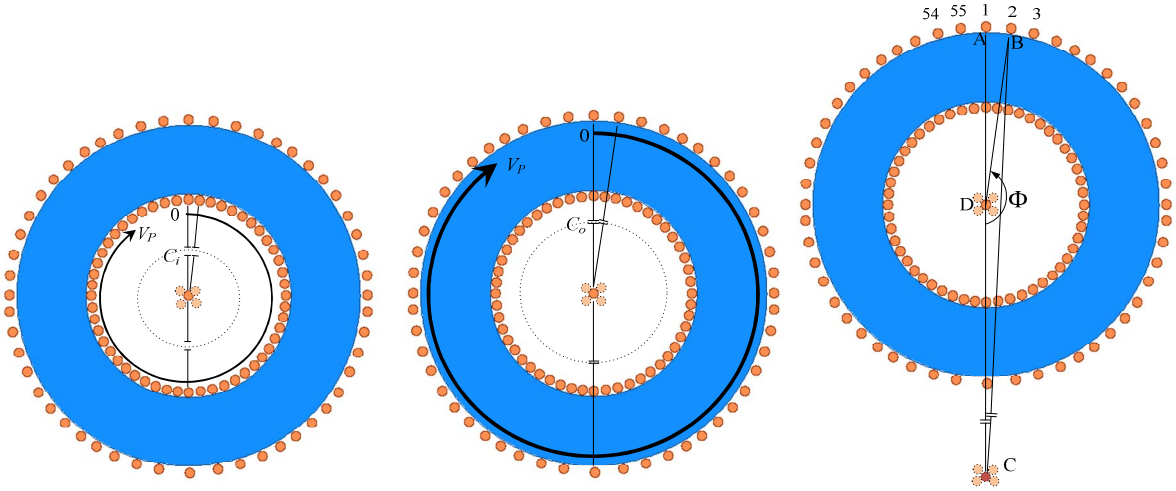
where ε_o is the permittivity of free air space, d is the diameter of each turns (the same size of wire is selected for both primary and secondary turns), l and r are the overlapped length and the distance between the inner primary turns and the secondary turns, respectively.

With respect to the outer primary turns, the static capacitance can be expressed with a different distance r_o,

$$C_o = \frac{\varepsilon_0 S}{r_o} = \frac{\varepsilon_0 d\pi l}{2r_o}. \tag{6}$$

Assuming that the voltage potential distribution along the primary turns varies linearly,

$$V_P[i] = \frac{i}{n_P - 1} V_P. \quad (\text{i}=0,1,2,3,\ldots n_P\text{-}1) \tag{7}$$



(a) (b) (c)

Fig. 7. 2-D cross-sectional top view: effect of parasitic capacitance from the secondary winding of a) segment A to the inner primary winding, b) segment A the outer primary winding, c) segment C to the outer primary winding

Then the total stored electric energy between all secondary turns and the inner primary turns is:

$$E_i = \frac{1}{2} C_i \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1}\right)^2$$

$$= \frac{1}{4} C_i \cdot \left[\frac{V_p^2 \cdot n_s \cdot n_p \cdot (2n_p - 1) \cdot}{3 \cdot (n_p - 1)} + \frac{V_s^2 \cdot n_p \cdot n_s \cdot (2n_s - 1)}{3 \cdot (n_s - 1)} - V_p \cdot V_s \cdot n_p \cdot n_s\right]. \quad (8)$$

With the same analytical approach, the total stored electric energy between all secondary turns and the outer primary turns can be achieved:

$$E_o = \frac{1}{4} C_o \cdot \left[\frac{V_p^2 \cdot n_s \cdot n_p \cdot (2n_p - 1) \cdot}{3 \cdot (n_p - 1)} + \frac{V_s^2 \cdot n_p \cdot n_s \cdot (2n_s - 1)}{3 \cdot (n_s - 1)} - V_p \cdot V_s \cdot n_p \cdot n_s\right]. \quad (9)$$

The capacitance caused by the side segments B_1, B_2 to the primary winding is:

$$C_B = \frac{\varepsilon_0 d \pi l_B}{2 r_B}. \quad (10)$$

Segments B_1 and B_2 face the middle parts of the primary winding. It is appropriate to assume that there are five turns from the primary winding, which lie in segment P_3 or P_4 of Fig. 6c, facing segment B_1 and B_2 respectively. They are turn number $(n_P-1)/2-2$, $(n_P-1)/2-1\ldots$ to $(n_P-1)/2+2$. For example, in a specific design with 55 primary turns, or $n_P = 55$, they will correspond to turn number 25 to 29. The stored electric energy caused by B_1 and B_2 is:

$$E_B = 2 \cdot \left(\frac{1}{2} C_B \sum_{j=0}^{n_S-1} \sum_{i=(n_P-1)/2-2}^{(n_P-1)/2+2} \left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1} \right)^2 \right). \quad (11)$$

Next, the contribution of segment C of the secondary winding to the outer ring of the primary winding is computed. Referring to Fig. 7c, it is helpful to express the distance from point C to the turns lying in the outer ring of the primary mathematically. In triangle CDB, distance $\overline{\mathrm{CB}}$ is related to other sides of the triangle by:

$$\overline{\mathrm{CB}}^2 = \overline{\mathrm{CD}}^2 + \overline{\mathrm{BD}}^2 - 2\overline{\mathrm{CD}}\,\overline{\mathrm{BD}}\cos(\Phi)$$

$$= (r_i + r_0)^2 + r_o^2 - 2(r_i + r_0) r_0 \cos(\pi - 2\pi / n_P). \quad (12)$$

Therefore, distance from C to the i^{th} turn of the outer-primary winding is (see Fig. 7c)

$$r_{Cout,i} = \sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o (r_o + r_i) \cos(\pi - \frac{i2\pi}{n_P})}. \quad (i = 0,1,2,3,\ldots,n_P - 1) \quad (13)$$

The capacitance from segment C of the secondary winding to the turn number i^{th} of the outer primary winding is:

$$C_{Cout,i} = \frac{\varepsilon_o d\pi l_c}{2r_{Cout,i}} = \frac{\varepsilon_o d\pi l_c}{2\sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_P})}}. \quad (i = 0,1,2,3,...,n_P - 1) \tag{14}$$

The total stored energy caused by segment C of secondary winding to the outer side of primary winding is then:

$$\begin{aligned} E_{Cout} &= \frac{1}{2}\sum_{j=0}^{n_S-1}\sum_{i=0}^{n_P-1} C_{Cout,i}\left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1}\right)^2 \\ &= \frac{1}{2}\sum_{j=0}^{n_S-1}\sum_{i=0}^{n_P-1} \frac{\varepsilon_o d\pi l_c}{2\sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_P})}}\left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1}\right)^2. \end{aligned} \tag{15}$$

Similarly, the stored energy caused by segment C of secondary winding to the inner side of primary winding is:

$$E_{Cin} = \frac{1}{2}\sum_{j=0}^{n_S-1}\sum_{i=0}^{n_P-1} C_{Cin,i}\left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1}\right)^2, \tag{16}$$

where

$$C_{Cin,i} = \frac{\varepsilon_o d\pi l_c}{2\sqrt{r_i^2 + (r_o + r_i)^2 - 2r_i(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_P})}}. \quad (i = 0,1,2,3,...,n_P - 1) \tag{17}$$

The total stored electric energy is then

$$E_{total} = E_i + E_o + E_B + E_{Cin} + E_{Cout} = \frac{1}{2}\cdot C_{eq}\cdot(V_p - V_s)^2. \tag{18}$$

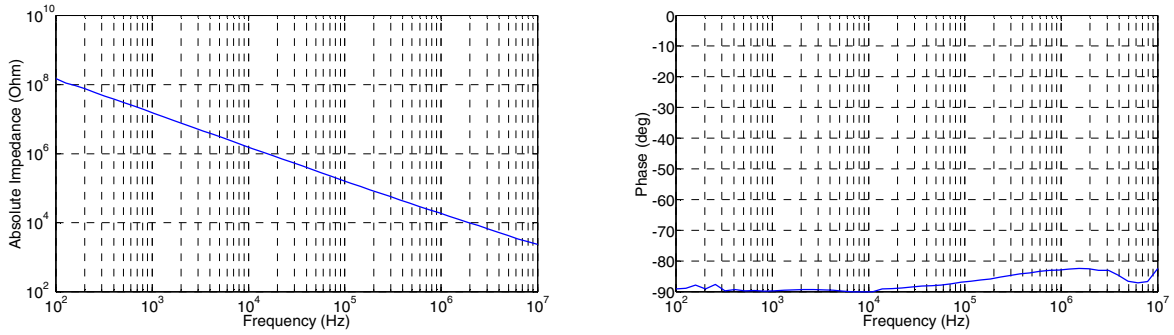
The calculated inter-winding capacitance based on the parameters on Table I is 10 pF. Table II shows the calculated energy and capacitance. It is observed that segment A_1 dominates the stored energy, and the contributions of segments B_1 and B_2 are negligible. The design guideline is that increasing the core geometry and increasing distance from segment C to the core will effectively reduce the inter-winding capacitance.

Table I: Parameters of the magnetic core and winding geometries

ε_0	8.85×10^{-12} F/m
d	1 mm
l	16 mm
r_i	11.5 mm
r_o	18 mm
n_p	55
n_s	11
V_p	300 V
V_s	60 V
r_B	12 mm
l_B	6.5 mm
l_c	16 mm

Table II: Calculated energy and inter-winding capacitance

Parameters	E_i	E_o	E_B	E_{Cin}	E_{Cout}	E_{total}	C_{eq}
Value	1.3e-7 J	8.4e-8 J	1.1e-9 J	3.8e-8 J	3.2e-8 J	2.9e-7 J	9.97e-12 F
$/E_{total}$	45.9%	29.3%	0.4%	13.1%	11.3%	100%	



(a) (b)

Fig. 8. Inter-winding impedance measurement: a) magnitude, b) phase.

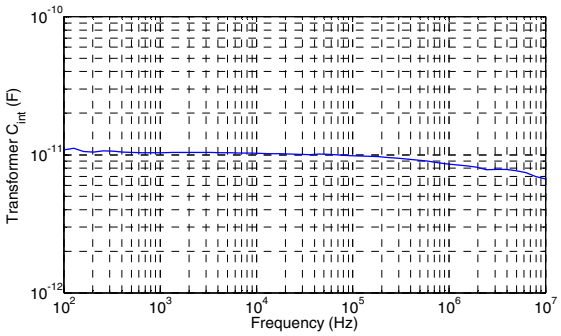


Fig. 9. Interpreted parasitic capacitance.

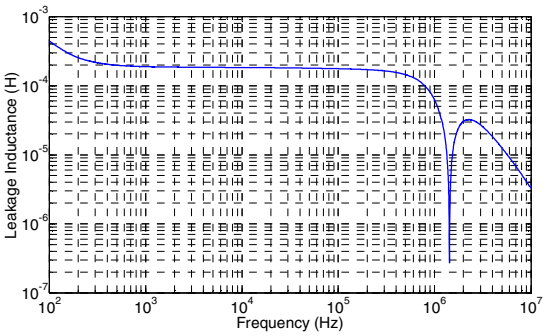
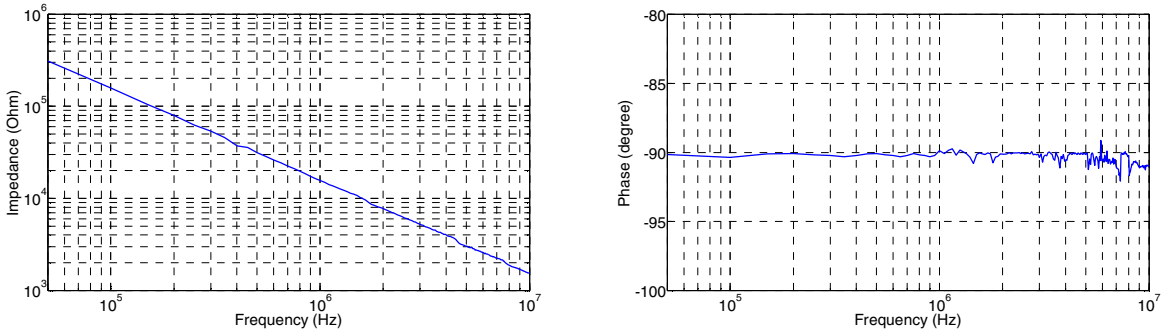


Fig. 10. The leakage inductance.



(a) (b)

Fig. 11. Circuit input-to-output impedance measurement Left: magnitude, Right: phase.

Experimental results

The measurement of the transformer is carried out by the Agilent 4294A Precision Impedance Analyzer, which has a precision of ±3 % as claimed by the manufacturer. The measured impedance and phase between the primary and secondary windings, with each winding terminal shorted, are shown in Fig. 8. The measured inter-winding capacitance is shown in Fig. 9. It is shown that the measured capacitance is around 10 pF from 3 kHz up to 10 MHz. The calculation and the measurements, are therefore, matched reasonably well with each other. The resulting leakage inductance is 170 µH, which is shown in Fig. 10. In the end, the overall design goal is fulfilled, which is to have a very low inter-winding capacitance of 10 pF. Fig. 11 shows the impedance magnitude and phase of the circuit. These were found by measuring the impedance between the input and the output terminals of the converter with the input and output shorted to their own return grounds. The measured circuit input-to-output parasitic capacitance is deduced from these measurements and is shown in Fig. 12. Its value is 10 pF, the same as with the inter-winding capacitance of the transformer. As a result, it can be said that the proposed circuit layout, control, and transformer design has minimized the total circuit input-to-output capacitance, making it a powerful solution for modular stacking applications. Finally, Figs. 13 and 14 show the experimental operation from power mode to shunt mode and from shunt mode to power mode. It can be seen that experiments match very well to the analysis presented in the circuit operation section. The feasibility of the converter is therefore validated.

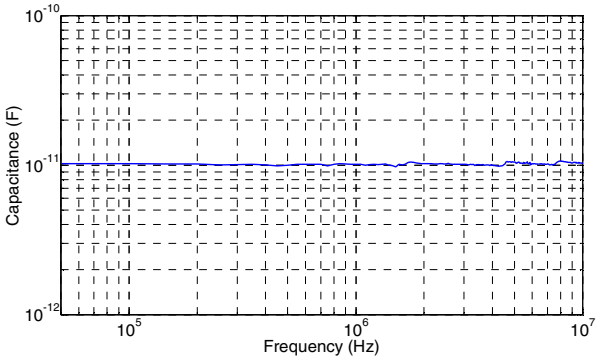


Fig. 12. Circuit input-to-output parasitic capacitance.

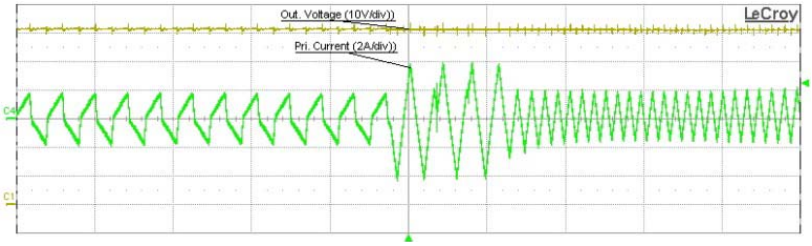


Fig. 13. Transient response from power mode to shunt mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div).

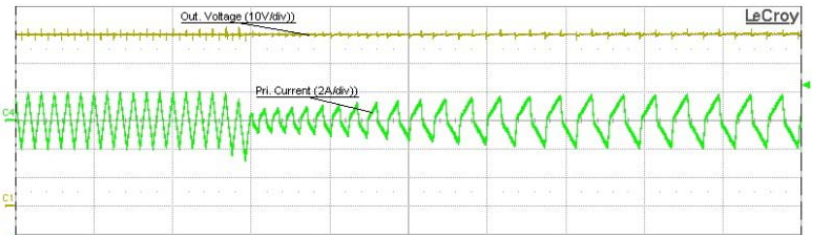


Fig. 14. Transient response from shunt mode to power mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div).

Conclusion

The resulting transformer has a parasitic capacitance of 10 pF, which is extremely low compared to other existing isolated power converters of similar power rating. The mathematical derivation yields acceptably accurate results that agree well with measurement. The results also provide guidelines about how the transformer geometry should be considered when the inter-winding capacitance is of concern. Finally, the overall result achieved with the prototype provides very high immunity to the common mode noise current caused by fast voltage transients, and therefore makes the converter suitable for modular stacking applications.

References

[1] M. A. E. Andersen.: MOS gate driver circuit with extremely high galvanic isolation, EPE 1995. Sevilla, Spain, vol. 1, p. 747-751.

[2] S. Wang, P. Kong and F. C. Lee.: Common mode noise reduction for boost converters using general balance technique, IEEE Trans. Power Electron., vol. 22, no. 4, pp.1410 -1416, Jul. 2007

[3] J. Biela and J. W. Kolar.: Using transformer parasitics for resonant converters—A review of the calculation of the stray capacitance of transformers, IEEE Trans. Ind. Appl., vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[4] L. Dalessandro, F. S. Cavalcante, and J. W. Kolar.: Self-capacitance of high-voltage transformers, IEEE Trans. Power Electron., vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[5] H.-Y. Lu, J.-G. Zhu, and S. Y. R. Hui.: Experimental determination of stray capacitances in high frequency transformers, IEEE Trans. Power Electron., vol. 18, no. 5, pp. 1105–1112, Sep. 2003.

[6] Z. Ouyang, O. C. Thomsen and M. A. E. Andersen.: Optimal design and tradeoff analysis of planar transformer in high power dc–dc converters, IEEE Trans. Ind. Electron., vol.59, no.7, pp.2800-2810, July 2012.

[7] T. Duerbaum and G. Sauerlaender.: Energy based capacitance model for magnetic devices, in Proc. IEEE Appl. Power Electron. Conf. Expo., pp.109-115, 2011.

[8] D. Garabandic, D. W.G. Dunford, M. Edmunds.: Zero-voltage-zero-current switching in high-output-voltage full bridge PWM converters using the interwinding capacitance, IEEE Trans. Power Electron., vol.14, no.2, pp.343,349, Mar 1999.

[9] K. Pengju and F.C. Lee.: Transformer structure and its effects on common mode EMI noise in isolated power converters, Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, pp.1424,1429, 21-25 Feb. 2010.

[10]M. Hoyerby and M. A.E. Andersen.: Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control, IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2387-2398, Sept. 2008.

[11]C. In-Ho, K. Young-Do and M. Gun-Woo.: A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation, IEEE Trans. Power Electron., vol. 29, no. 2, pp .841-850, Feb. 2014.

[12]H. Manli, J. Bocker and N. Frohleke.: Frequency / duty cycle current-mode fuzzy control for LCC resonant converter," 2011 - 14th European Conference on Power Electronics and Applications (EPE), Aug. 30 2011-Sept. 1 2011.

[13]D. Costinett, D. Maksimovic, D.; R. Zane.: Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency, IEEE Trans. Power Electron., vol.28, no. 8, pp. 3931-3940, Aug. 2013.

[14]G. Guidi, A. Kawamura, Y. Sasaki and T. Imakubo.: Dual active bridge modulation with complete zero voltage switching taking resonant transitions into account, 2011 - 14th European Conference on Power Electronics and Applications (EPE), Aug. 30 2011-Sept. 1 2011.

[15]A. Garcia-Bediaga, A. Rujas, I. Villar, P. Barrade and A. Rufer, A.: New parametric model of medium-frequency single-active-bridge converters, 2013 - 15th European Conference on Power Electronics and Applications (EPE), 2-6 Sept. 2013

[16]P. Kiwoo and C. Zhe.: Analysis and design of a parallel-connected single active bridge DC-DC converter for high-power wind farm applications, 2013 - 15th European Conference on Power Electronics and Applications (EPE), 2-6 Sept. 2013

[17]EPCOS.: SIFERRIT material N87, Sept. 2006, available:http://www.epcos.com/blob/528882/download/3/pdf-n87.pdf

A.5 (PEAC2014)-Loss Performance Analysis of an Isolated Power Supply for Ultrafast Tracking Converters

Paper A.5. is entitled "Loss Performance Analysis of an Isolated Power Supply for Ultrafast Tracking Converters." Presented in The IEEE International Power Electronics and Applications Conference and Exposition (PEAC2014), Shanghai, China, 5-8 November 2014.

Loss Performance Analysis of an Isolated Power Supply for Ultrafast Tracking Converters

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***Abstract*—This paper presents the loss performance analysis of an isolated power supply that is designed for ultra-fast tracking converters. The results of the analysis provide insights into the operation of the proposed power supply, how each physical component contributes to the total loss, and how its efficiency may be further improved.**

Keywords—Dc-dc power converters, loss measurement, magnetic losses, switching loss.

I. Introduction

Power supply designed for fast output voltage transient applications should meet certain requirements regarding their input-to-output parasitic capacitance. Specifically, the circuit input-to-output capacitance should be as low as possible in order to mitigate the transmission of common mode noise generated by the fast output voltage transients [1]-[4]. First, [1] proposed an isolated power supply with a power rating of 36 V/5 W and a ring core transformer with an inter-winding capacitance of 1 pF. Next, [2], [3], and [4] introduced a prototype using the same topology as in [1], but the power rating was increased to 60 V/300 W and the proposed transformer had an inter-winding capacitance of 10 pF.

Reference [2] and [3] also described the circuit operation, control, and general structure of the proposed transformer in addition to the circuit topology. However, the loss performance analysis of the converters had not been addressed. The topology introduced in [1] and studied in [2]-[3] is shown in Fig. 1.

This paper addresses the loss performance analysis of the converter proposed in [1]-[4]. The detail of the circuit operation will not be covered in this paper; they can be found in [2] and [3]. Instead, this paper will focus on the loss performance of the converter prototype proposed in [3]. It will be shown that the loss calculation matches well with the experiments. The results suggest how each physical component contributes to the total loss, and how its efficiency may be further improved.

II. Converter Operation and Its Influence on Individual Loss

The converter proposed in [2], [3] and studied in this paper for its loss performance is shown in Fig. 1. The specification of the prototype is shown in Table I. It consists of a full-bridge

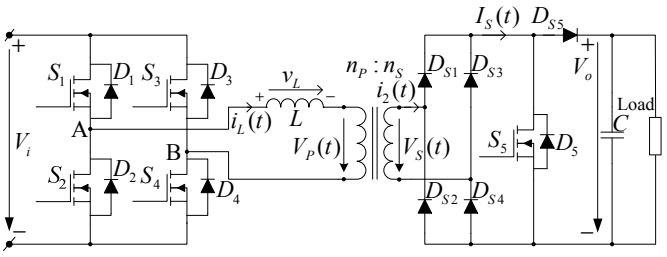
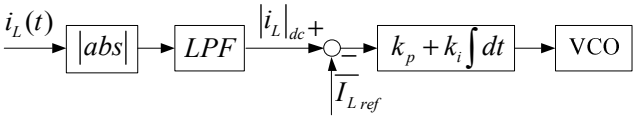


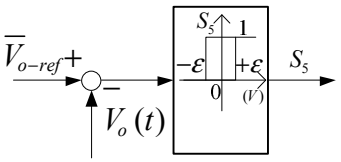
Fig. 1. The topology of the proposed power supply.

TABLE I. Prototype Specification

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Leakage inductance	170 µH



(a)



(b)

Fig. 2. Control block diagram. (a) Average current mode control in the primary side and (b) hysteresis control in the secondary side.

on the primary side and a proposed shunt regulator on the secondary side. The two sides are linked by a transformer that has an extremely low interwinding capacitance of 10 pF. This makes the power supply suitable for supplying energy to applications with fast changes in voltage such as the ultrafast tracking converters. Because of the transformer winding structure that minimizes the interwinding capacitance, the resulting leakage inductance L is large, which is 170 µH [3]. This inductance is used as the main energy storage component to transfer current from the primary to the secondary side. There is no external inductor added to the circuit structure except for the leakage inductor of the proposed transformer.

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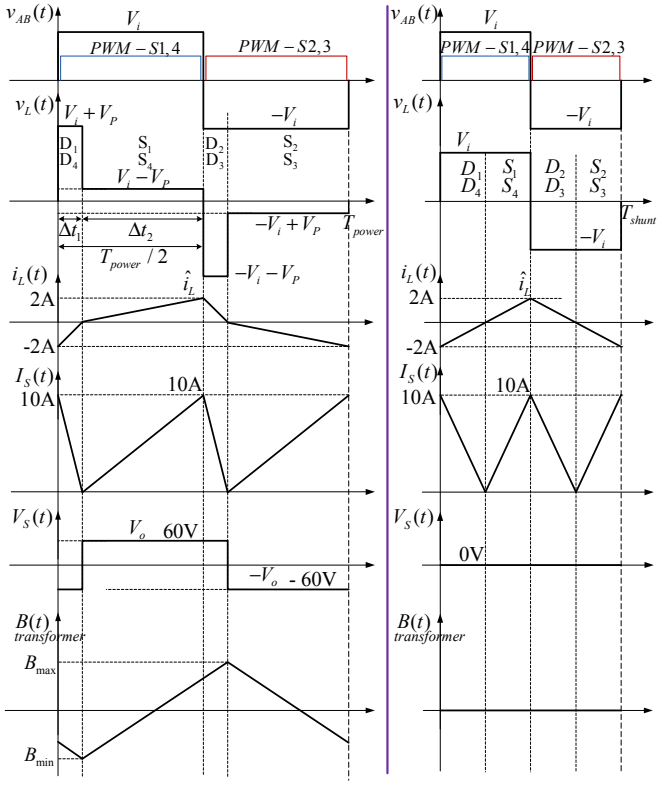

Fig. 3. Analytical waveforms when the converter operates in: (a) Power mode and (b) shunt mode.

The converter circuit operation is briefly sated in this section. The detail can be found in Section VI of [3]. It is very important to understand different operation modes of the proposed converter in order to analyze the individual loss.

There are two control loops whose block diagrams are shown in Fig. 2. The secondary side controller regulates the output voltage to be constant at 60 V. The output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch ON and OFF the shunt switch S_5.

When S_5 is OFF, the converter operates in its *power mode*, which is shown in Fig. 3(a); the output voltage increases because the output current $I_S(t)$ supplies energy to the load. Vice versa, when S_5 is ON, shunting the secondary side, the converter operates in its *shunt mode* (see Fig. 3(b)); the output voltage decreases because the secondary current I_S(t) is isolated from the load. On the primary side control, the primary side current i_L is sensed. It is rectified and filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analog proportional-integrator (PI) controller. The output of the PI controller is fed to a voltage-controlled oscillator (VCO) that will automatically adjust the switching frequency to keep the rectified primary dc current to be constant at 1 A dc. The duty cycle of the primary switches is regulated at 50 %. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc.

When the converter operates in power mode, the output power is 300 W because the output current $I_S(t)$ which has a dc value of 5 A is supplying the load whose voltage is regulated at 60 V dc. On the other hand, when the converter operates in shunt mode, the output current $I_S(t)$ is isolated from the load, circulating through S_5; the output power is zero. The converter is constantly switching between the power mode and shunt mode. It depends on the output power level to determine how long the converter is operating in each mode. For example, if the converter is desired to deliver 300 W at the output, then it will fully operate in power mode. If the converter is desired to shut down the output power, or to not deliver any power at all, then the converter will entirely operate in shunt mode. The higher the output power (closer to 300 W) the longer time the converter operates in power mode.

Therefore, if the converter outputs a power of P_{out}, then the duty cycle in which the converter operates in power mode will be:

$$d_{power} = \frac{P_{out}}{P_{\max}}, \tag{1}$$

where P_{max} is the maximum output power of the converter. In this design, P_{max} is equal to 300 W. Likewise, the duty cycle in which the converter operates in shunt mode is:

$$d_{shunt} = \frac{P_{\max} - P_{out}}{P_{\max}} = 1 - d_{power} \tag{2}$$

Duty cycle d_{shunt} is also the duty cycle of turning-on shunt switch S_5. It is noticed that d_{power} and d_{shunt} changes with output power.

During shunt mode, the switching frequency of the primary side switches, f_{shunt}, is 307 kHz. During power mode, the switching frequency, f_{power}, is 124 kHz. The detail of the derivation of the switching frequency can be found in Section VI of [3].

The switching between the two operation modes affect different individual loss in a different way because the current waveforms and switching frequency are switched between two modes. The losses that are affected by the switching of the operation modes are the switching losses of the primary side switches, the core loss and copper loss of the transformer, and the losses in D_{S5} and S_5. For convenience, for the losses calculation involving the switching frequency, the normalized switching frequency is introduced:

$$f_{norm} = d_{power} f_{power} + d_{shunt} f_{shunt}. \tag{3}$$

It is also noticed that f_{norm} changes with the change in output power. For example, $f_{norm} = f_{power}$ when $P_{out} = P_{\max}$, and $f_{norm} = f_{shunt}$ when $P_{out} = 0$.

On the contrary, the transition between the two operation modes does not affect the conduction losses of the primary side switches S_1—S_4 and the conduction loss of the diode

bridge consisting of D_{S1}—D_{S4}. This is because the currents flowing through these devices do not change their root-mean-square value regardless of the operation mode as shown in Fig. 3. This will also be observed in the next section from the formulas used to calculate these conduction losses.

III. Loss Performance Analysis

A. Losses on the Primary Side Switches S_1—S_4

The power dissipation of primary side MOSFETs consists mainly of conduction loss and switching loss:

$$P_{d\_total} = P_{d\_cnd} + P_{d\_sw}, \tag{4}$$

where P_{d_total} is the total loss in the four primary switches, P_{d_cnd} is the total conduction loss, and P_{d_sw} is the total switching loss. At any instant of a full switching period, there are maximum two MOSFETs conducting. Therefore, the conduction power loss in one primary side switch, $P_{cond-1MOS}$, is:

$$P_{cond-1MOS} = R_{DS-on} I_{rms}^2 = R_{DS-on} \left(\frac{I_{peak}}{\sqrt{3}} \sqrt{d}\right)^2, \tag{5}$$

where I_{rms} is the root-mean-square value of the current flowing through a primary switch during a period, I_{peak} is the peak current value, I_{peak} = 2 A, and d is the duty cycle of the current, d = 0.5 (see Fig. 4). R_{DS-on} is the on resistance of the drain to source of the MOSFET. R_{DS-on} = 1.1 Ω at 65°C and a gate-source voltage of 10 V. The power MOSFET on the primary side uses part IRF840 from Vishay whose datasheet can be found in [5].

From (5), the conduction loss does not change regardless of the operation mode in which the converter is operating. This is because the root-mean-square value of the current is the same in both modes. The total conduction loss in the whole four primary side MOSFETs, P_{d_cnd}, is therefore:

$$P_{d\_cnd} = 4P_{cond-1MOS} = 2.93 \text{ W}. \tag{6}$$

At the turning-on transitions of the MOSFETS, the transitions are made from the body diode in the same MOSFET to its channel. For example, the transition are from D_1 to S_1, D_2 to S_2, D_3 to S_3, and D_4 to S_4. Because the MOSFETs are conducting, the voltages across them are zero. It is also observed that the currents conducting through them are crossing the zero value. This characteristic can be observed from Fig. 4. For this reason, there is no switching loss in the turn-on transitions.

The total switching loss during turn off in the whole four MOSFET is:

$$P_{d\_sw} = 4P_{sw-1MOS} = 4E_{off} f_{sw} = 2V_i I_{peak} t_f f_{norm}, \tag{7}$$

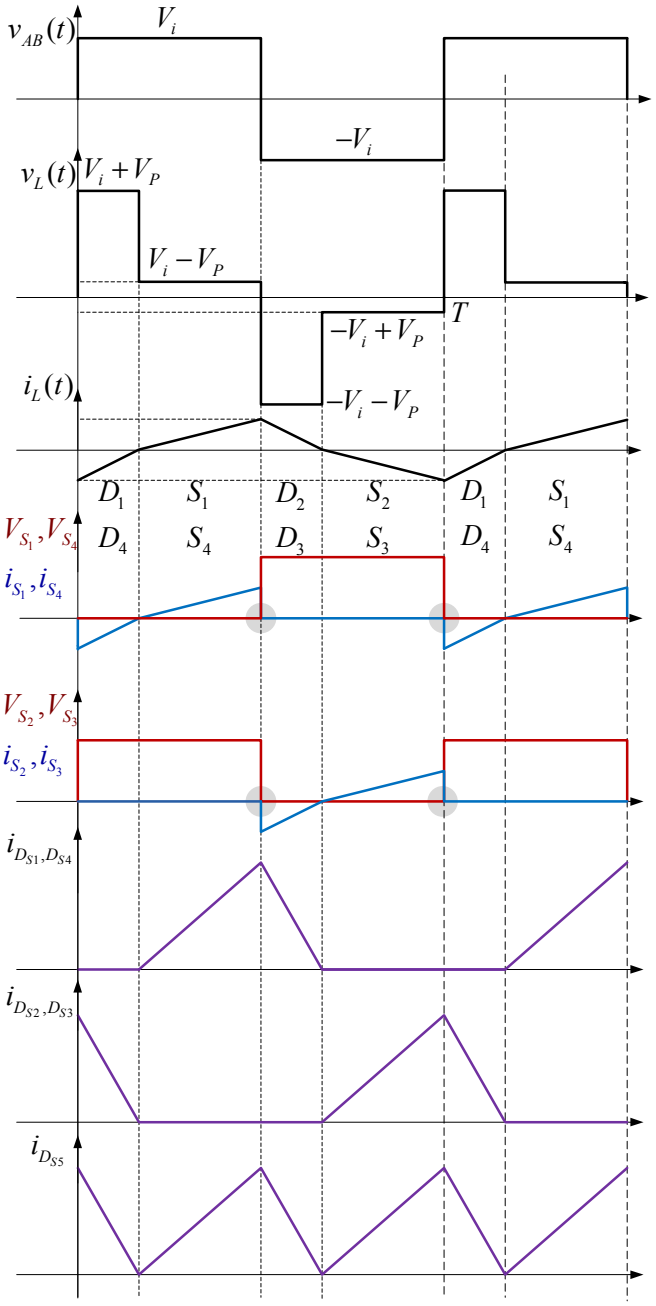

Fig. 4. The current and voltage waveforms across power switches and diodes.

where E_{off} is the energy loss during turn-off transients, I_{peak} is the peak current value during turn-off, and t_f is the fall time duration provided by the datasheet of the MOSFET, t_f = 30 ns.

B. Losses on the Secondary Side

1) Loss in the diode bridge D_{S1}—D_{S4}

The diode bridge uses part MBR10T100 from Vishay [6]. The loss in one diode, P_{1-D}, is:

$$P_{1-D} = V_{FM} I_{D-avg} + R_D I_{D-rms}^2, \quad (8)$$

where V_{FM} is the forward voltage drop. Its value is V_{FM} = 0.57 V at 125°C and 0.71 V at 25°C. The value of V_{FM} at 65°C is used in the calculation because the prototype is attached to two sufficiently large heat sinks that are expected to keep the temperature rise of the power switches to be within 40°C Taking the linear interpolation of V_{FM} yields V_{FM} = 0.65 V. R_D is approximated to be equal to the slope the diode current-voltage curve at the average operating forward current of 5 A. From the data-sheet of the part used, the value of R_D is 0.02 Ω. This value is taken into the loss estimation. Meanwhile, I_{D-avg} is the average value of the current flowing through each diode, I_{D-avg} = 2.5 A. I_{D-rms} is the root-mean-square value of the diode current, $I_{D-rms} = (I_{D-peak} / \sqrt{3})\sqrt{d_D}$. The duty cycle of the triangular current flowing through one diode is d_D = 0.5. The peak diode current value is I_{D-peak} = 10 A. Therefore, I_{D-rms} = 4.1 A.

Substituting these values to (8) yields P_{1-D} = 1.96 W. The total loss in the four diodes in the rectifier bridge is:

$$P_{D-bridge} = 4P_{1-D} = 7.83 \text{ W}. \quad (9)$$

It is noted that there is no reverse-recovery loss in the diode bridge since the diode parts are Schottky-effect diodes.

2) Loss in forward diode D_{S5}

Forward diode D_{S5} also uses part MBR10T100 from Vishay [6]. The forward average current flowing through diode D_{S5} is: $I_{DS5-avg}$ = 5 A (see Fig. 4). The root mean square of that current is: $I_{DS5-rms} = (I_{DS5-peak} / \sqrt{3})\sqrt{d_{DS5}}$ = 5.8 A, where d_{DS5} is the duty cycle of the current, d_{DS5} = 1, $I_{DS5-peak}$ is the current peak value, $I_{DS5-peak}$ = 10 A. The forward voltage drop is V_{FM} = 0.65 V at 65°C. The value of R_D is 0.02 Ω.

The loss in forward diode D_{S5} is therefore:

$$P_{DS5} = V_{FM} I_{DS5-avg} + R_D I_{DS5-rms}^2 = 3.92 \text{ W}. \quad (10)$$

3) Loss in shunt MOSFET S_5

Shunt MOSFET S_5 uses part IRF540 from Vishay [7], which has an on-resistance of 0.096 Ω at 65°C at a gate-source voltage of 10 V. The conduction loss is:

$$P_{DS5} = R_{S_5-DS-on} I_{S_5-rms}^2 = 3.2 \text{ W}, \quad (11)$$

where I_{S_5-rms} is the root-mean-square value of the current flowing through S_5 during shunt mode.

Because the switching frequency of S_5 is small, the switching loss is small compared to the conduction loss and is ignored.

C. Losses in the Transformer

TABLE II. PARAMETERS OF MAGNETIC CORE AND WINDING GEOMETRIES OF THE TRANSFORMER

Material	N87
Dimension	36 mm × 23 mm × 15 mm
Turns ratio	55 : 11
Primary winding	Litz-wire 60 × 0.2 mm
Secondary winding	Copper 1 mm diameter
Effective cross sectional area	A_e = 95.89 mm^2
Effective volume	V_e = 8597 mm^3

TABLE III. FITTING COEFFICIENT OF THE CORE LOSS CALCULATION

K_{Fe}	25.2156
x	1.2786
y	2.5850
f_{eq}	0.81 f

The parameters of the magnetic core and material, and turns ratio are listed in Table II. The parameters of the magnetic core geometries and material characteristic can be found in [8] and [9], respectively. The detailed description of the transformer structure can be found in [3] and it will not be covered again in this paper.

According to the Modified Steinmetz Equation (MSE) reported in [10]-[16], the core loss per volume, P_{Fe-rel}, is:

$$P_{Fe\_rel} = K_{Fe} f_{eq}^{x-1} \hat{B}^y f, \quad (12)$$

where K_{Fe}, x, and y are dependent on the core material. K_{Fe}, x, and y are based on Steinmetz equation and they can be extracted from curve-fitting the experimental ferrite loss in the datasheet in [9]. $\hat{B}$ is the peak flux density, f is the switching frequency, and f_{eq} is the equivalent switching frequency. According to [10], f_{eq} is related to the switching frequency f and the shape of the flux density waveform by

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt} \right)^2 dt, \quad (13)$$

where ΔB is the peak-to-peak value of the flux density, T is the period of the excitation. The equivalent switching frequency, f_{eq}, is equal to f if sinusoidal excitation is used.

In this converter, the excitation is based on a triangular wave form as shown in the bottom of Fig. 3. From (13), we have

$$\begin{aligned} f_{eq} &= \frac{2}{(2\hat{B})^2 \pi^2} \left(\int_0^{T/2} \left(\frac{2\hat{B}}{T/2} \right)^2 dt + \int_{T/2}^{T} \left(\frac{2\hat{B}}{T/2} \right)^2 dt \right) \\ &= \frac{2}{4\hat{B}^2 \pi^2} \left(\frac{16\hat{B}^2}{T^2} t \Big|_{t=0}^{t=T/2} + \frac{16\hat{B}^2}{T^2} t \Big|_{t=T/2}^{t=T} \right) \\ &= \frac{8}{\pi^2 T} = \frac{8}{\pi^2} f = 0.81 f. \end{aligned} \quad (14)$$

The results of these fitting coefficients are shown in Table III, where P_{Fe_rel} is in watt per cubic-meter.

The calculated core loss is P_{Fe} = 2.39 W. The calculated copper loss is 2.13 W in power mode and 2.97 W in shunt mode.

IV. Experimental Results

The prototype of the proposed power supply is shown in Fig. 5. Fig. 6 shows the transient response from power mode to shunt mode. In a similar way, the transient from shunt mode to power mode is shown in Fig. 7. The value of the output voltage threshold, ε, is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady state values, which are 2 A peak and 60 V dc, respectively. The transient of the current from power mode to shunt mode and vice versa finishes within about 30 µs and 40 µs, respectively. The time needed for the inductor current to settle is mainly determined by the dynamic of the average current control scheme described in Fig. 2(a). Nevertheless, the transient and steady state are both stable and satisfactory. The behavior of the circuit matches accurately with the aforementioned circuit analysis.

The calculated break down loss is shown in Fig. 8. As can be seen, the loss in the primary side H-bridge accounts more than 60 % of the loss at low output power and around 40 % at high output power. The loss contributed by the diode bridge is constant because both the average and the root mean square value of the current flowing through the bridge is constant. The loss created by the forward diode D_{S5} and the shunt MOSFET S_5 is small compared to the loss in the H-bridge and the diode bridge. The loss in the transformer is also small compared to the dominant losses which are losses in the H-bridge and the diode bridge. As output power reduces, the duration in which the converter operates in shunt mode increases linearly. Even though the losses in the combination of forward diode D_{S5} and the shunt MOSFET S_5 and in the transformer decrease with the decrease of output power, their rate of decrease is smaller than the rate of increase in the switching loss of the primary side switches. Therefore, the total loss increases with lower output power. Thus, the efficiency drops.

The measured and calculated total loss are shown in Fig. 9. The power measurement is carried out by the PPA5530 precision power analyzer. The accuracy claimed by the manufacturer is ±0.4 % in the operation condition under test. It can be seen that the calculated total loss and the measured total loss match very well with each other. The largest discrepancy between the calculated loss and measured loss is 1.9 W at 222 W output power. This discrepancy constitutes 7.5 % difference between the calculated and measured total loss and 0.85 % difference between the calculated efficiency and the measured efficiency. One of the reasons that explain this discrepancy could be the accuracy of the precision power analyzer used. Nevertheless, the calculated total loss is able to predict the trend of the total loss. It is asymptotical to the measured total loss. It has been proven that the loss is approxi-

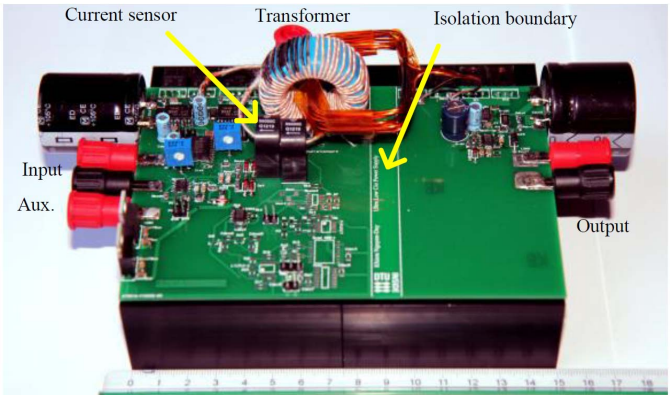

Fig. 5. A photo of the prototype of the proposed converter.

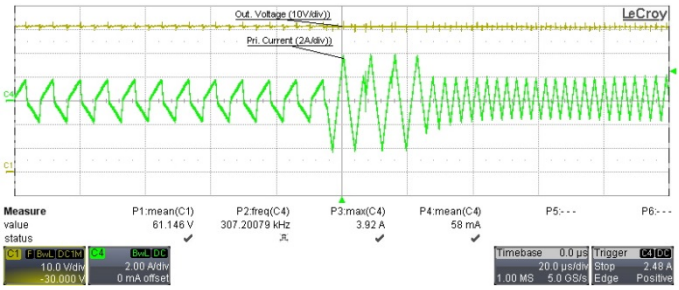

Fig. 6. Transient response from power mode to shunt mode. Top: output voltage (10V/div); bottom: inductor current (2A/div); time scale: 20 µs/div).

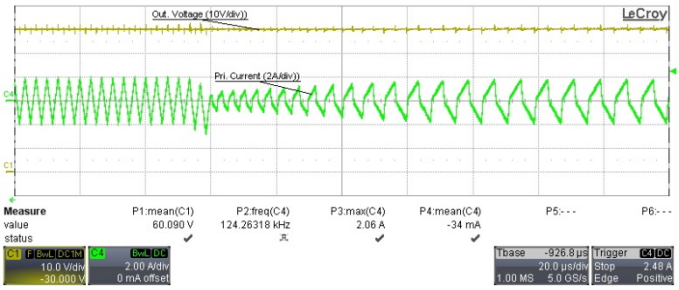

Fig. 7. Transient response from shunt mode to power mode. Top: output voltage (10V/div); bottom: inductor current (2A/div); time scale: 20 µs/div).

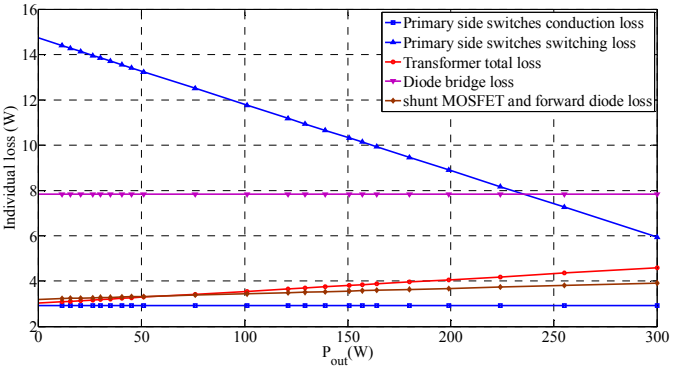

Fig. 8. Calculated breakdown loss.

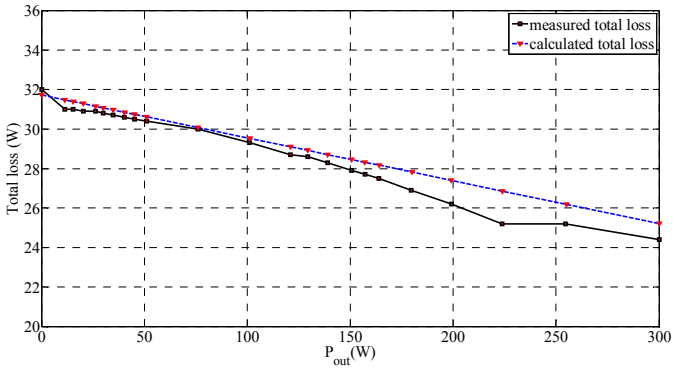

Fig. 9. Measured and calculated total loss.

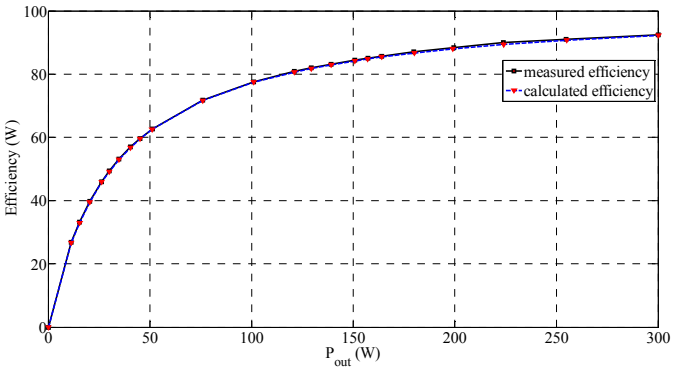

Fig. 10. Measured and calculated efficiency.

mated to be a linear combination of the shunt mode loss and power mode loss, as described in Section II.

The highest efficiency is 92.4 %, which is shown in Fig. 10. In general, the overall efficiency of the converter is satisfactory particularly in the range of 1/3 of the nominal power to the nominal power. The efficiency in this range is from 77.5 % to 92.4 %.

The calculated results show that the primary side switching loss is the predominant loss in the converter. Therefore, in order to further improve the efficiency of the converter, it is suggested that future design focus on reducing the switching loss on the primary side. It may be achieved by selection of different MOSFET part that is faster and hence yields lower switching loss.

V. Conclusion

This paper has dealt with the loss performance analysis of a novel power supply specially designed for ultra-fast tracking converters. The methods of calculating loss associated with each major physical device have been presented. The calculated total losses have been proven to match well with the measured data. The results of this analysis can serve as a guidance about which physical elements should be taken into account when the overall efficiency is of concern.

References

[1] M. A. E. Andersen, “MOS gate driver circuit with extremely high galvanic isolation,” in *Proc. Eur. Conf. Power Electron. Appl.*, *1995*, pp. 747—751.

[2] K. Nguyen-Duy, L. P. Petersen, A. Knott, O. C. Thomsen, and M. A. E. Andersen, "Design of a 300-Watt isolated power supply with minimized circuit input-to-output parasitic capacitance," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drive*, pp. 1—6,April 8—10, 2014.

[3] K. Nguyen-Duy, Z. Ouyang, L. P. Petersen, A. Knott, O. C. Thomsen, and M. A. E. Andersen, "Design of a 300-W isolated power supply for ultrafast tracking converters," in Early Access, *IEEE Transactions on Power Electronics,* vol., no. 99, pp.1,1.

[4] K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, “Minimization of the transformer inter-winding capacitance for modular stacking power supply applications,” in *Proc. 16th Eur. Conf. Power Electron. Appl.,* 26–28, Aug. 2014.

[5] (2014). VISHAY IRF840, SiHF840 Power MOSFET. [Online]. Available: http://www.vishay.com/docs/91070/91070.pdf

[6] (2007, Oct.). VISHAY MBR10T100 High Performance Schottky Generation 5.0, 10A. [Online]. Available: http://www.farnell.com/datasheets/39509.pdf

[7] (2011, Mar.). VISHAY IRF540, SiHF540 Power MOSFET. [Online]. Available: http://www.vishay.com/docs/91021/91021.pdf

[8] (2006, Sep.). EPCOS Ferrites and accessories, Toroids R 30.5, R 34.0, R 36.0, Series/Type B64290. [Online]. Available: http://www.epcos.com/inf/80/db/fer_07/r_30.pdf

[9] (2006, Sep.). EPCOS Ferrites and accessories, SIFERRIT material N87. [Online]. Available: http://www.epcos.com/blob/528882/download/3/pdf-n87.pdf

[10] J. Reinert, A. Brockmeyer, and R.W. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp.1055—1061, Jul/Aug 2001.

[11] J. Reinert, A. Brockmeyer, and R.W. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," in *Proc. 34th Ind. Appl. Conf.*, vol. 3, no., pp. 2087—2092, 1999.

[12]W. A. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *IEEE Transactions on Power Electronics,* vol. 22, no. 1, pp. 30—40, Jan. 2007.

[13]M. Popescu, D. M. Ionel, A. Boglietti, A. Cavagnino, C. Cossar, and M. I. McGilp, "A general model for estimating the laminated steel losses under PWM voltage supply," *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1389—1396, July-Aug. 2010.

[14]J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Transactions on Power Electronics,* vol. 27, no. 2, pp. 964—973, Feb. 2012.

[15] A. Van den Bossche, V. C. Valchev, and G. B. Georgiev, "Measurement and loss model of ferrites with non-sinusoidal waveforms," in *Proc. 35th Power Electron. Specialists Conf.*, vol. 6, no., pp. 4814—4818, 20-25 June 2004.

[16] P.-K, Lee, K.-C. Kuo, C.-J. Wu, Z.-T. Wong, and J.-T. Yen, "Prediction of iron losses using the modified Steinmetz equation under the sinusoidal waveform," in *Proc. 8th Asian Control Conf.* (ASCC), pp. 579—584, 15-18 May 2011.

A.6 (ELEKTRONIKA2014)-Constant Switching Frequency Self-Oscillating Controlled Class-D Amplifiers

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Constant Switching Frequency Self-Oscillating Controlled Class-D Amplifiers

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***Abstract*—The self-oscillating control approach has been used extensively in class-D amplifiers. It has several advantages such as high bandwidth and high audio performance. However, one of the primary disadvantages in a self-oscillating controlled system is that the switching frequency of the amplifier varies with the ratio of the output voltage to the input rail voltage. In other words, the switching frequency varies with the duty cycle of the output. The drop in the frequency results in lower control bandwidth and higher output voltage ripple, which are undesirable. This paper proposes a new self-oscillating control scheme that maintains a constant switching frequency over the full range of output voltage. The frequency difference is processed by a compensator whose output adjusts the total loop gain of the control system. It has been proven by simulation that a constant switching frequency self-oscillating converter is achieved and the proposed control circuit performs satisfactorily.**

***Index Terms*—Power amplifiers, frequency control, voltage control, power electronics.**

I. INTRODUCTION

Switch mode class-D audio amplifiers have been replacing the audio amplifiers made from class-A, B or AB amplifiers thanks to their superior efficiency and power density [1]–[5]. For the control of class-D audio amplifiers, the modulation strategy is an integral factor that determines the performance of the audio amplifiers. Modulation strategies can be classified into analogue modulation and digital modulation.

The analogue modulation usually has better performance due to the absence of digital delay or quantization error, which are inherent in digital modulation [6]. There have been two basic analogue modulation methods in the literature, namely the triangular carrier-based modulation method and the self-oscillating control method. The self-oscillating control method uses a comparator with either hysteresis [7], [8] or zero-hysteresis [9].

Recently, the self-oscillating control method has received great attention due to its advantages over the triangular carrier based method [6]–[13]. The advantage of the self-oscillating control system is that it allows the open-loop control system magnitude to cross the 0 dB point precisely

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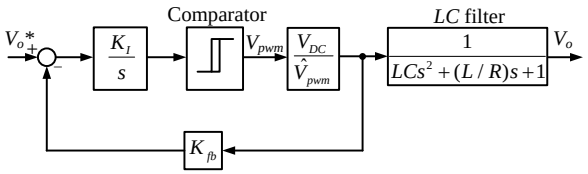

Fig. 1. A basic voltage-mode hysteresis controller.

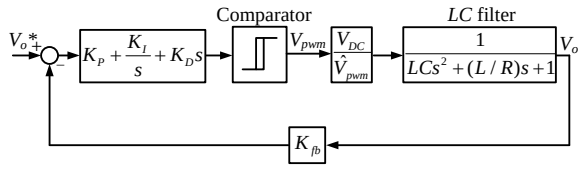

Fig. 2. A global loop integrating modulator controller.

at the oscillation frequency, providing high control bandwidth. On the other hand, the cross over frequency of the carrier-based modulation control system must be at least several times lower than the switching frequency, resulting in lower bandwidth and higher output ripple.

Figure 1 introduces a basic voltage-mode, hysteresis-based, self-oscillating control system. The output filter is a second-order *LC* filter. The switching node of a synchronous buck converter is fed back and compared with the voltage reference, which, in the case of audio amplifiers, is a reference for the audio output signal. K_{fb} is the feedback constant of the switching signal. The rail voltage is V_{DC} with respect to ground for a single supply converter, or can be from $+V_{DC}/2$ to $-V_{DC}/2$ for dual supply audio amplifiers. For consistency, a single supply voltage is assumed. In the control scheme, the integrator amplifies the error and provides infinite gain at dc. The phase shift created by the integrator is –90°. The negative feedback of the signal provides a phase shift of –180°. The remaining phase shift is provided by the nature of the hysteresis comparator, the time delay of gate driver, and the propagation of the control units. Assuming there is no other time delay produced by the other physical elements in the control loop, the hysteresis comparator provides –90° phase shift at the nominal switching frequency.

Figure 2 shows another hysteresis-based, self-oscillating control system for class-D amplifiers. It feeds back the output voltage instead of the switching signal. This scheme

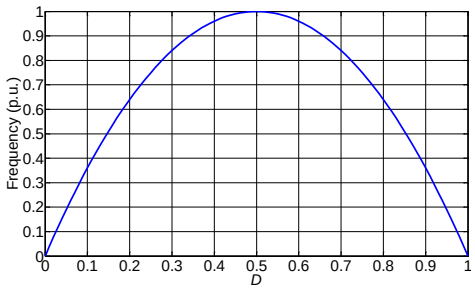

Fig. 3. Frequency (normalized to the maximum frequency) versus changes of duty cycle.

is usually referred to as the Global Loop Integrating Modulator (GLIM) scheme [12]. Since the transfer function of the output filter is taken into the control loop, the integrator in Fig. 1 is replaced by a proportional-integral-derivative (PID) controller. The PID controller cancels out the two poles created by the output filter and provides high dc gain with its integral term. The PID controller, together with the output filter, can be approximately treated as an integral, making the open loop transfer function similar to that in Fig. 1. The advantage of this scheme compared to the basic scheme in Fig. 1 is that the errors from both the output voltage and output filter are attenuated [12].

However, a major problem with the self-oscillating control system applied in class-D amplifiers is that the switching frequency varies with the duty cycle of the output stage. The variation is based on a parabolic curve with peak value at a duty cycle of 0.5. This is due to the decrease in the gain when the duty cycle is different from 0.5. From previously published papers, it can be shown that the switching frequency has the following expression [6]–[8]

$$f_{sw} = \frac{K_{sw} D(1-D)}{\varepsilon}, \qquad (1)$$

where ε is the height of the hysteresis threshold (hysteresis window), K_{sw} is a constant dependant on the circuit gain, and D is the duty cycle. In the case of a single supply system, the modulation index is defined by the proximity of the output signal V_o, which is biased by half the rail supply voltage, to the closest supply rail. Thus, the modulation index is defined as

$$M = \frac{|V_o - V_{DC}/2|}{V_{DC}/2} = |2D-1|. \qquad (2)$$

The *centre duty cycle* is the duty cycle that produces the maximum frequency in a self-oscillating controlled system. In this case, the centre duty cycle is D = 0.5. A plot of the switching frequency, normalized to the maximum frequency, versus the change in duty cycle is shown in Fig. 3. It can be seen that the frequency drops rapidly with the change of duty cycle away from the centre duty cycle. For example, when the duty cycle is 0.1 or 0.9, the switching frequency drops 64 %, or nearly two thirds from the nominal frequency.

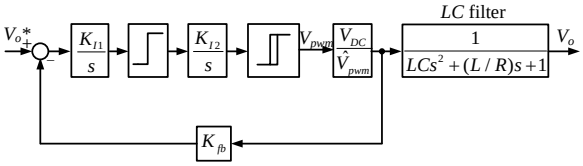

Fig. 4. The fixed frequency self-oscillating control system proposed in [6].

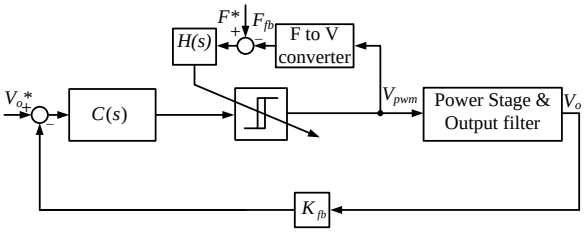

Fig. 5. The fixed frequency self-oscillating control system proposed in [8] and [13].

This drop in the switching frequency is undesirable because it results in several undesired consequences. First, the drop of the switching frequency increases the output voltage ripple. Second, the drop causes the open-loop bandwidth and loop gain to drop as well, resulting in higher distortion and slower dynamics. As a result, it is desired that the switching frequency in self-oscillating controlled systems be fixed at the nominal frequency in order to counteract the aforementioned drawbacks.

Based on the independence of the switching frequency to the threshold and the gain, as shown in equation (1), the switching frequency can be fixed by either altering the gain [6] or online-adjusting the hysteresis threshold [2], [7], [8], [13]. Between these approaches, the later has dominated.

In [6], the frequency is fixed by modifying the control loop. Specifically, a second integrator is inserted into the circuit together with a second comparator. The control scheme is redrawn in Fig. 4. The drawback is that the switching frequency is nearly but not exactly constant.

The methods proposed in [8] are very similar to those in [13], wherein the frequency is converted to voltage, which is then processed by a high gain compensator. The output of the high gain compensator is used directly to adjust the hysteresis window through, for example, a flip-flop circuit. The only difference between [8] and [13] is that the method in [8] is applied to a different type of converter, namely the buck converter with a fourth-order output filter. However, ideas proposed in [13] also includes phase compensation by use of a phase-lock-loop circuit, unlike [8]. Their control block diagram is redrawn in Fig. 5, where *C(s)* is a generalized compensator for the output voltage, and *H(s)* is the aforementioned high gain compensator.

Reference [2] introduces the concept of fixing the frequency by adjusting the hysteresis threshold from the output of a compensator that processes feed-forward input reference signals or feedback PWM signals. However, the discussion of this concept in [2] is general, and there is neither proper analysis nor associate evidence to support its claims.

This paper seeks to solve the problem in a different way. Similar to [6], the hysteresis threshold ε will be fixed.

However, the gain of the open loop control system is adjusted by a feedback control of the frequency signal, so that the whole open loop gain crosses the 0 dB point at the desired switching frequency. The compensating gain will be injected to the open loop system via a multiplication unit (multiplier). The detailed description of the proposed method will be presented next.

II. PROPOSED CONSTANT SWITCHING FREQUENCY CONTROLLER

In the studied system, a rail voltage of 60 V dc is used to supply the power stage. The converter is a synchronous buck converter. The nominal load is 26 Ω. The nominal switching frequency is 1 MHz. The specifications of the converter to be examined are listed in Table I.

The proposed fixed-frequency, self-oscillating control system is shown in Fig. 6. The PWM signal generated by the hysteresis comparator is converted to a voltage proportional to its frequency. This is done by passing the PWM to a mono-stable multi-vibrator (MMV) or one-shot circuit with a fixed pulse width output. Each time the input to the MMV has a rising edge, the output of the MMV generates a pulse with a fixed width, which is 100 ns in this case. The resulting signal of the MMV is low-pass filtered by a first order *RC* filter circuit with a cut-off frequency of 1.6 kHz. Only the dc value of the MMV remains, and it is proportional to the switching frequency. The operation of the MMV and the F-to-V converter are illustrated in Fig. 7 and Fig. 8.

The measured switching frequency is compared to the reference switching frequency and processed by a compensator *F(s)*. *F(s)* can be implemented with a PI or PID controller. The output of *F(s)* is the compensating gain for the self-oscillating control loop, and it is inserted to the control loop through a multiplier. It adjusts the switching frequency of the converter to track the reference frequency, which is represented by *F**.

III. SIMULATION RESULTS

The simulation studies examine different responses of the converter using the self-oscillating control approach without frequency compensation as well as with the proposed frequency compensation. The responses are based on both dc reference signals and sinusoidal audio reference signals. Simulation model was built in MATLAB®/Simulink environment. Most parts of the controllers and feedback were modelled and simulated by realistic commercially available discrete components: non-ideal operational amplifiers with limited gain-bandwidth product and limited output voltage ability, etc.

A. Converter without a Frequency Compensator

Figure 9 shows the voltage transient (step) response of the converter without a frequency compensator. The dc reference values are swept so that the duty cycle of the output voltage is changed. At time t = 0, the duty cycle is 0.5. At times t = 70 μs, t = 140 μs, t = 210 μs, the duty cycle is 0.2, 0.1, and 0.7, respectively. The bottom of Fig. 9 shows the switching signal generated by the comparator. It can be seen that the switching frequency varies with the change of the duty cycle. Its peak value is at the centre frequency where D = 0.5. This phenomenon can be observed more clearly from a partial zoom of Fig. 9 which is shown in Fig. 10.

TABLE I. THE SPECIFICATION OF THE CONVERTER.

Parameter	Value
L	36 μH
C	100 nH
V_{DC}	60 V
V_{pwm}	5 V
ε	0.66 V
Nominal load	26 Ω
Nominal switching frequency	1 MHz
t_{MMV}	100 ns

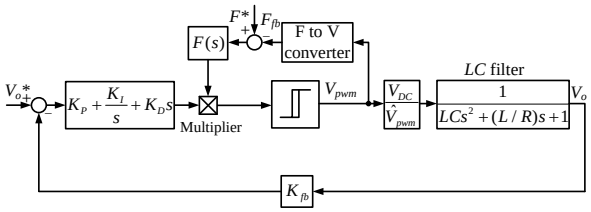

Fig. 6. The proposed fixed frequency self-oscillating control system.

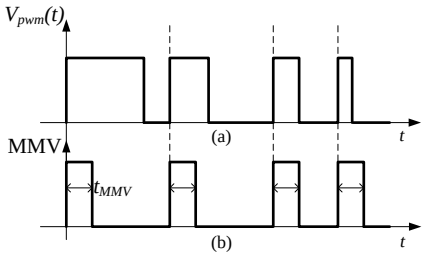

Fig. 7. Operation of the MMV a) the PWM output signal of the comparator, b) the output signal of the mono-stable multi-vibrator.

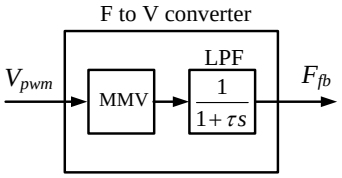

Fig. 8. Frequency to voltage (F to V) converter.

Figure 11 shows response to an audio signal of the conventional converter without a frequency compensator. The frequency of the signal is 20 kHz, which represents an audio signal for typical human hearing ability. It can be confirmed again from the simulation result, that the switching frequency varies with the magnitude of the audio signal, or in other words, it varies with the switching duty cycle. As Fig. 3 suggests, the drop of the frequency at higher modulation index creates larger output ripple and distortion. This phenomenon can be observed from the top and bottom of the output voltage signal.

B. Converter with the Proposed Frequency Compensator

Figure 12 shows the step response of the self-oscillating control amplifier with the proposed frequency compensator.

As can be seen, the switching frequency of the converter in steady state held constant regardless of the variation in the output voltage or duty cycle. The steady-state response of the output voltage has been improved, while a desirable transient response is preserved. The ripple of the output voltage is reduced at all switching duty cycles that are different from the centre duty cycle. This feature can be seen in the partial zoom of Fig. 12 shown in Fig. 13.

Converter without a frequency compensator is shown in Fig. 9–Fig. 11.

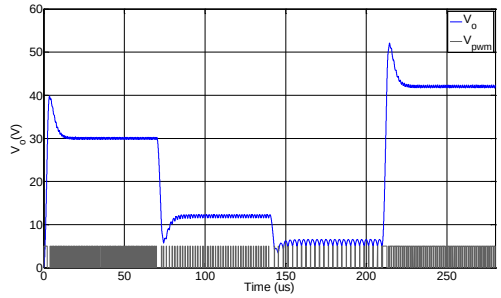

Fig. 9. Step response of output voltage without a frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is swept from 0.5 to 0.2, 0.1, and 0.7.

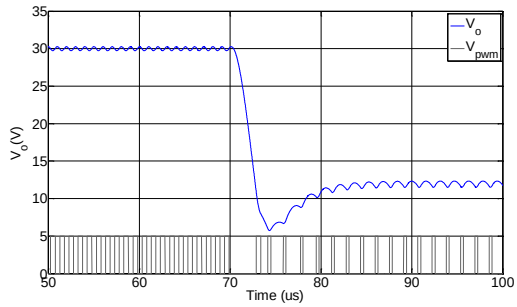

Fig. 10. Partial zoom of the step response of output voltage without a frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is shifting from 0.5 to 0.2 at time 70 µs.

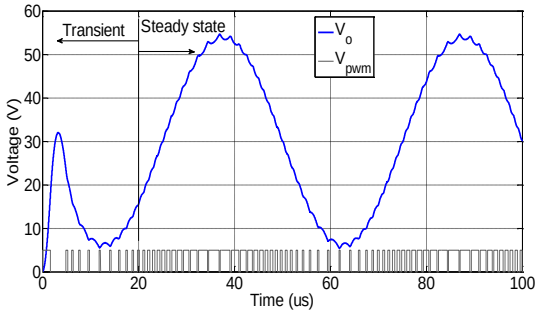

Fig. 11. Output response to a 20-kHz audio reference without a frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is continuously varying from 0.1 to 0.9 and vice versa.

The response to an audio input signal of 20 kHz is presented in Fig. 14. It can be seen that the switching frequency of the converter has been held constant even with a large variation in the duty cycle over one period. The ripple at the top peak and bottom peak of the output signal, therefore, has been significantly improved compared to Fig. 11. The amplifier with the proposed constant-frequency compensator outperforms the traditional one without a frequency compensator. Different simulations are performed with both converters at various duty cycles. The switching frequencies are plotted in Fig. 15 for four cases: calculated by equation (1), simulated model without a frequency compensator, simulated model with the proposed frequency compensator, and simulated model with method proposed in [6]. As can be seen, the simulated switching frequency without a frequency compensator matches well with the calculation. Moreover, a constant switching frequency is guaranteed with the proposed method.

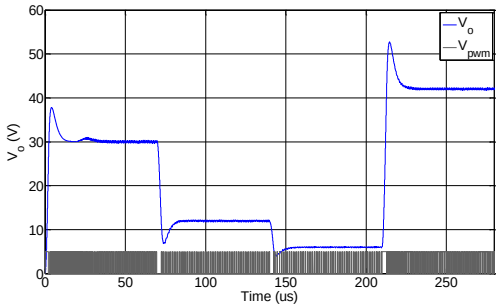

Fig. 12. Step response of output voltage with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is swept from 0.5 to 0.2, 0.1, and 0.7.

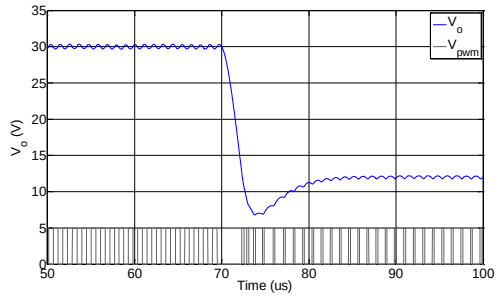

Fig. 13. Partial zoom of the step response of output voltage with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is shifting from 0.5 to 0.2 at time 70 µs.

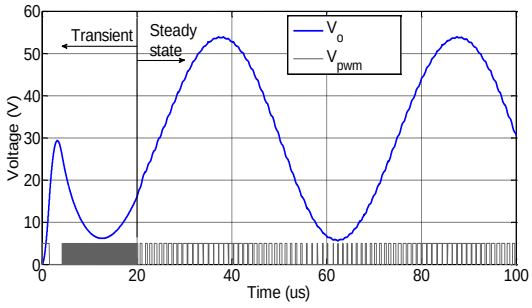

Fig. 14. Output response to a 20-kHz audio reference with the proposed frequency compensator. Top: V_o (V), bottom: V_{pwm} (V), the duty cycle is continuously varying from 0.1 to 0.9 and vice versa.

Converter with the proposed frequency compensator is shown in Fig. 12–Fig. 14.

IV. DISCUSSION

While most existing solutions for fixing the switching frequency have worked with varying the hysteresis window when the duty cycle changes, the approach presented here fixes the hysteresis window and generates a compensating gain based on the variation in frequency.

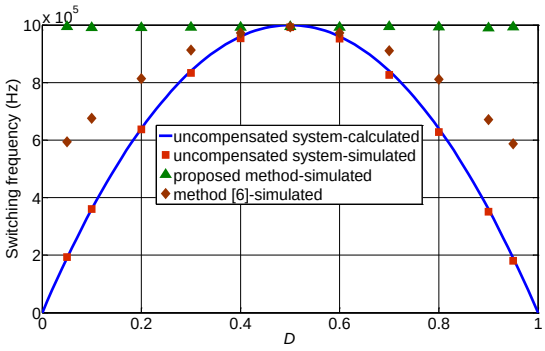

Fig. 15. Switching frequency versus variation of duty cycle: calculated results without frequency compensation, simulated results without frequency compensation, simulated results with the proposed frequency compensation, and simulated results with the method proposed in [6].

In [6], the hysteresis window is kept constant and the regulation of frequency is achieved by changing the loop gain. The added integrator is implemented by a passive *RC* filter. Therefore, the low frequency gain is preserved, but the high frequency components are attenuated. The extra comparator differentiates the output of the added integrator, yielding clamped output signals. Therefore, the gain of the low frequency signal is preserved at the rate of –20 dB/dec, ensuring a linear carrier signal to the main comparator, while the high frequency signals are approximately attenuated with a slope of –40 dB/dec. As a result, a drop of gain due to a change of modulation index will result in half of the drop in the switching frequency compared to the uncompensated system. In fact, that method is only able to reduce the drop of the switching frequency by approximately half compared to an uncompensated system. Finally, the article also states that only "close to constant switching frequency" is achieved. The advantage of this method is its simplicity and low-cost compared to the method proposed in this paper.

In [7], the comparator is configured with positive feedback to yield hysteresis. The novelty of this method is to use feedback impedance, which consists of frequency dependant components such as an *RC* network instead of passive resistors. The network is used to filter out the PWM signals generated by the comparators. When the duty cycle diverges from the centre value, the filtered signal has a smaller value, providing a higher gain to compensate the drop of term *D(1-D)* in equation (1). However, the compensated gain is only dependant on the impedance magnitude of the *RC* network, which proves to vary differently from the desired parabolic gain of *D(1-D)*. The method is only valid at a specific value of the output duty cycle, and cannot guarantee a constant switching frequency over the whole output range. In fact, the frequency is only raised for different modulation indexes, but it fails to be raised at very high modulation index. As a result, only "close to constant switching frequency" is claimed. The advantage is simple and low-cost implementation by means of insertion of passive resistors and capacitors.

The methods in [8] and [13], due to their direct compensation of either frequency errors or phase errors, have the advantage of precise control of the desired switching frequency. The penalties of those methods are high complexity and component count if implemented by analogue components.

Compared to the known existing methods analysed above, the proposed method has high precision frequency control for similar reasons as in [8] and [13]. However, the significant differences are the compensation mechanism and the method of implementation. The proposed method focuses on compensating the drop of open loop gain by providing a correcting gain and injecting it to the self-oscillating loop. Conversely, the methods in [8] and [13] adopt the classical approach of changing the hysteresis threshold. Implementation of adjusting the hysteresis threshold must involve extra effort to design the comparator circuit with fast online tuning capability of the hysteresis threshold. On the other hand, implementation of the proposed compensator can be less complex, involving a good dynamic multiplication unit while allowing the use of standard comparators.

V. CONCLUSIONS

In this paper, the authors have proposed a new approach to maintain constant switching frequency of self-oscillating controlled converters. It has been proven by extensive simulation studies that the proposed idea is effective. The proposed methods not only preserve the fast transient response characteristic of a self-oscillating controlled system, but also improve the steady state response by lowering the output voltage ripple. The feasibility of the idea can be verified with experiments in a future work.

REFERENCES

[1] ELBO GmbH, "Selbstshwingender digitalverstärker", DE 198 38 765 A1, German patent, May 2000.

[2] A. Veltman, J. J. Hendrikus, "Amplifier circuit", WO 00/42702, Int patent, January 2000.

[3] A. F. Rozman, J. J. Boylan, "Band pass current control", in *Conf. Proc. IEEE (APE 1994)*, pp. 631–637, vol. 2, 1994.

[4] F. C. Lee, R. P. Iwens, Y. Yu, "Generalized computer-aided discrete time domain modelling and analysis of dc-dc converters", in *Conf. Rec. PESC 77*.

[5] K. Nielsen, J. L. Hansen, "Synchronized controlled oscillation modulator", WO 03/055060 A1, Int. patent, July 2003.

[6] S. Poulsen, M. A. E. Andersen, "Hysteresis controller with constant switching frequency", *IEEE Trans. Consumer Electronics*, vol. 51, no. 2, pp. 688–693, 2005.

[7] K. Hyoung-Sik, J. Sung-Wook, J. Hwan-Mok, S. Jang-Kyoo, C. Pyung, "Low cost implementation of filterless class-D audio amplifier with constant switching frequency", *IEEE Trans. Consumer Electronics*, pp. 1442–1446 vol. 52, no. 4, 2006.

[8] M. Hoyerby, M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control", *IEEE Trans. Power Electronics*, vol. 23, no. 5, pp. 2387–2398, 2008.

[9] A. Huffenus, G. Pillonnet, N. Abouchi, F. Goutti, V. Rabary, C. Specq, "A phase-shift self-oscillating stereo class-D amplifier for battery-powered applications", in *Conf. Proc. 2010 IEEE Int. Sym. Circuits & Systems (ISCAS)*, 2010, pp. 769–772.

[10] L. Jingxue, R. Gharpurey, "Design and analysis of a self-oscillating class-D audio amplifier employing a hysteretic comparator", *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2336–2349, 2011.

[11] F. A. Malekzadeh, R. Mahmoudi, A. Roermund, "Statistical analysis of self-oscillating power amplifiers", *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1865–1876, 2011.

[12] S. Poulsen, "Global loop integrating modulator", WO2004100356-A2, patent application.

[13] D. Grant, "Frequency control of hysteretic power converter by adjusting hysteresis levels", U.S. patent 6,348,780.

A.7 (IEEE-TPEL JOURNAL)-High Dynamic Performance Nonlinear Source Emulator

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High Dynamic Performance Nonlinear Source Emulator

Khiem Nguyen-Duy, *Student Member, IEEE,* Arnold Knott, *Member, IEEE,*
and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—As research and development of renewable and clean energy based systems is advancing rapidly, the nonlinear source emulator (NSE) is becoming very essential for testing of maximum power point trackers or downstream converters. Renewable and clean energy sources play important roles in both terrestrial and non-terrestrial applications. However, most existing NSEs have only been concerned with simulating energy sources in terrestrial applications, which may not be fast enough for testing of non-terrestrial applications. In this paper, a high bandwidth NSE is developed that is able to simulate the behaviors of a typical nonlinear source under different critical conditions that can happen during their operations. The proposed 200-W NSE, which consists of a fourth-order output filter buck converter and a novel nonlinear small signal reference generator, can quickly react not only to an instantaneous change in the input source but also to a load step between nominal and open circuit. Moreover, all of these operation modes have a very fast settling time of only 10 μs, which is hundreds of times faster than that of existing works. This attribute allows for higher speed and a more efficient maximum power point tracking algorithm. The proposed NSE, therefore, offers a superior dynamic performance among devices of the same kind.**

***Index Terms*—Current-voltage characteristics, DC-DC power converters, energy resources, nonlinear circuits, renewable energy sources.**

I. Introduction

A. Background

The world is rapidly changing from using fossil based energy, which is facing exhaustion, to the use of renewable and clean energy sources, such as wind, sun, fuel cell energy, and battery power. In the testing and development phase of these energy sources, the use of nonlinear source emulators (NSE) offers many advantages over the use of their real counterparts. First, NSEs are compact, and do not require as large of a testing space as nonlinear sources such as wind turbines or PV panels. Second, the cost of a test system using NSEs is usually less than that of actual nonlinear sources [1]. Another example is that of non-rechargeable power batteries, which would have to be disposed of after each test; hence, testing would be expensive and extra care must be taken to not harm the environment [2], [3]. On the contrary, a battery emulator constructed from a power electronics converter can be reused for a long time and is not only cost effective but also friendly to the environment [4]–[8]. Finally, an NSE offers flexible and reproducible test conditions through their programmable set points. On the other hand, testing conditions of a real nonlinear source such as a PV or wind energy source are very difficult to be reproduced because of their dependency on weather, season, coverage, and time of the day of testing. With the many possible advantages that it can offer, the NSE has become an important and beneficial element in testing of power conditioning units. As a result, research on the development of NSEs has received great attention [2]–[13].

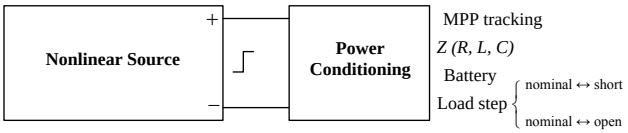

Fig. 1. Connection between a nonlinear source and a power conditioning unit.

A power conditioning unit that connects with a nonlinear source can take many different forms, which can be seen in Fig. 1. It can be a maximum power point (MPP) tracker that tracks the MPP of the nonlinear source. It can also be an impedance such as an ohmic load, an inductive load or a capacitive load. In addition, a power conditioning unit can also be a power battery that stores energy from the nonlinear source. It can also be a system that regulates average output voltage by applying a frequent load step between nominal load and short circuit, or a load step between nominal load and open circuit. In voltage regulation by means of load stepping, the system is pulse width modulated and switching with high frequency (20 kHz or more [14]). The two different types of load step will be presented in more detail later in the next subsection.

The static voltage-current relationship of a fuel cell system can be represented by a high-order polynomial as in [11], [12]:

$$V = f(I) = \alpha_3 I^3 + \alpha_2 I^2 + \alpha_1 I + \alpha_0, \tag{1}$$

where V is the fuel cell terminal voltage, I is the fuel cell output current, and α_0 to α_3 are the coefficients of the static

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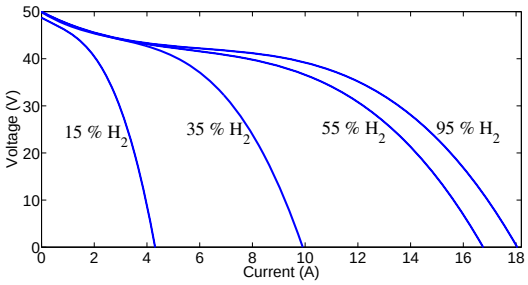


Fig. 2. Changes of dc operating point due to changes of hydrogen concentration levels in a fuel cell system [11], [12].

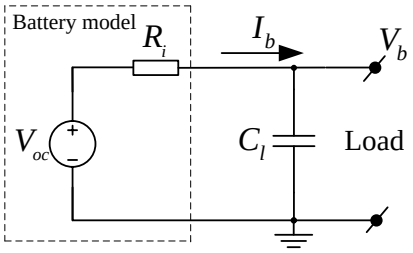


Fig. 3. A circuit model of a battery with load [2].

V-I curve; they change according to the change of hydrogen concentration. Fig. 2 shows an example of the static V-I curve characteristics of a fuel cell system at different hydrogen concentration levels. With each hydrogen concentration level of a specific fuel cell system, there exists a set of four coefficients α_0 to α_3 derived by means of curve fitting that can describe the system steady-state V-I curve.

There has not been any satisfactory equivalent electrical circuit developed that can closely describe the V-I relationship of a hydrogen fuel cell system because of its high nonlinearity. This is one of the reasons why nonlinear V-I reference curves in existing fuel cell emulators have always been implemented by digital control circuits such as digital signal processor (DSP) and field-programmable gate array (FPGA), in order to take advantage of their mathematical processing power [9]–[13].

Batteries are used extensively in industry such as in electric vehicle (EV) and hybrid electric vehicle (HEV) applications [2], [3], [7]. A circuit model of a battery is shown in Fig. 3. The dashed-line box models a battery, in which, V_{oc} and R_i are the open-circuit voltage and internal resistance, respectively. The rest of the circuit models an output with a filter capacitance C_l [2], [3]. The available voltage at the output of the battery is simply:

$$V_b = V_{oc} - IR_i. \tag{2}$$

During the discharge of the battery, V_{oc} decreases while R_i increases; both of them are dependent on the state of the battery and its internal temperature.

In the modeling of a PV panel, the *five-parameter model* [15], [16] is widely used to describe its electrical characteristic. The model is shown in Fig. 4. It is also called

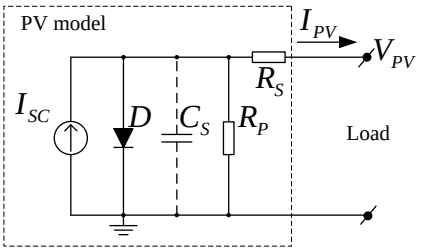


Fig. 4. The five-parameter model of a PV panel.

the *single diode model* [15]–[17]. The current is related to the terminal voltage V_{PV} and the short circuit current I_{SC} by:

$$I_{PV} = I_{SC} - I_o(\mathrm{e}^{(\frac{V_{PV}+I_{PV}R_S}{nV_t})} - 1) - \frac{V_{PV}+I_{PV}R_S}{R_P}. \tag{3}$$

In this model, R_P is the *parallel resistor* that models the loss due to manufacturing defects. R_S is the *series resistor* that models the loss due to mainly three causes: the movement of current through the emitter and base of the PV cell, the contact resistance between the metal contact and the silicon, and the resistance of the top and rear metal contacts [18]. I_o is the *dark saturation current* of the diode, which is the diode leakage current density in the absence of light. V_t is the *thermal voltage*, which is equal to approximately 25.85 mV at a temperature of 300 K. Parameter n is the *ideality factor* – a constant between 1 and 2 that depends on the manufacturing of the PV cell and may slightly vary with the operating point of it. For a given PV cell, the short circuit current I_{SC} is mainly determined by the intensity of the incident solar radiation, and the open circuit voltage V_{OC} is mainly determined by the cell temperature.

B. Dynamic Performance of Nonlinear Sources

The hydrogen concentration changes in fuel cell have quite a large time constant. According to [11], [12], this time constant is 10 s. In other words, it will take approximately 10 s for the voltage and current of a fuel cell to reach its steady-state under a change of hydrogen concentration performed by the fuel cell control system.

Furthermore, fuel cell systems have also quite a slow dynamic with regard to load changes [13]. Also according to [11], [12], the output impedance of a typical fuel cell system has a dominant pole at 20 Hz, which makes the output to react in the range of 50 ms or longer.

In short, fuel cell systems are rather slow systems. As a result, most of the challenges with developing a fuel cell emulator will lie on the digital control unit that calculates the nonlinear reference. On the other hand, from a control point of view, the power converter unit of a fuel cell emulator, which generates power, will not be much of a challenge due to its slow dynamic. It can be easily constructed by programmable off-the-shelf power supplies, such as the work in [11]–[13].

Among the aforementioned nonlinear sources, a PV system is the one that has the most critical demand for transient response. It is therefore the focus of this paper to develop

a fast response NSE that will be able to emulate the most speed-demanding system among the known nonlinear sources. Since it can emulate the fastest system, it will be capable of simulating any other types of nonlinear source after proper adjustments.

The five-parameter model is sufficient as long as the dynamic performance of a PV panel is not of critical concern. This is the case with existing PV emulators that are designed for terrestrial applications, where most of the time, the main focus is paid to the tracking of the MPP. In fact, the MPP changes with a rather slow speed. According to the survey conducted in [19], existing MPP tracking techniques in the literature have a moderate convergence speed of tens of milliseconds. That implies a requirement for the transient speed of the real PV panel or the PV emulator of approximately 10 Hz to 100 Hz. In fact, a nonlinear source can experience a frequent load step in some specific operation mode. This is where the dynamic response of a nonlinear source is exceptionally important. This is also where the model in Fig. 4 should take into account the PV panel's intrinsic source capacitance that is shown in dotted lines.

In practice, a real PV panel physically contains an intrinsic source capacitance due to the diffusion capacitance of each PV cell [20]. This capacitance is in parallel with the diode and the parallel resistor. The value of this capacitor varies with operating points of the PV panel. For example, existing work such as [20] reported that the value range of the source capacitance of a 312-W, 400×8 cm×cm silicon PV panel is from approximately 4 nF at the point close to the short circuit, to 6.7 μF at the open circuit. The data reported in [20] are plotted in Figs. 5 and 6.

The presence of the source capacitance plays a critical role in the determination of a PV panel's dynamic response. It makes the output current and voltage of a real PV panel under a load step to undergo a transient time in the range of tens of microseconds to settle down [14]. It is the time for the current source I_{SC} to charge the source capacitor C_S until the new operating voltage is reached. This can be verified by the following estimation. Supposing the converter is experiencing a load step; the operating point is moving from the short circuit to a resistive load that corresponds to the operating point of (V_o, I_o)= (160 V, 0.982 A), where the short circuit current is 1.07 A. Thus, $R = V_o/I_o$ = 163 Ω. From Fig. 6, the source capacitance is C_S = 107 nF. Considering a current source of I_{SC} = 1.07 A constantly supplies a load that consists of a source capacitance C_S of 107 nF in parallel with a resistive load R of 163 Ω, the output voltage as a function of time is:

$$v_o(t) = I_{SC}R(1 - \mathrm{e}^{\frac{-t}{RC_S}}). \tag{4}$$

The transient time for this PV system to move from short circuit $(0, I_{SC})$ to (V_o, I_o) is approximated by:

$$\Delta t = -RC_S ln(1 - \frac{V_o}{I_{SC}R}) = 4.37 \times 10^{-5}\ s = 43.7\ \mu s. \tag{5}$$

By the same approximation method, it will take approximately 1.1 μs for this PV system to complete the transition from the short circuit to the operating point (V_2, I_2)= (60 V, 1.062 A). In summary, it is proven that it will take the PV panel only microseconds to tens of microseconds to finish a transient. Notice that this dynamic is thousands of times faster than the dynamic of a typical fuel cell system, which is stated above to be in the range of tens of milliseconds to a few seconds.

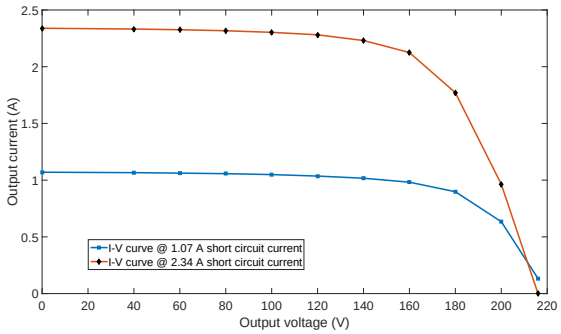


Fig. 5. I-V curve generated from measurement data in [20].

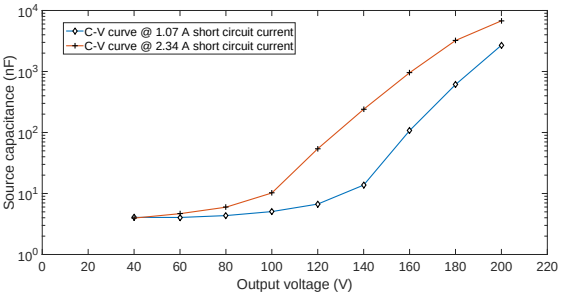


Fig. 6. C-V curve generated from measurement data in [20] .

Moreover, much more extreme conditions are usually met in non-terrestrial applications (such as PV panels attached to sky explorers) than those in terrestrial applications. First, a PV panel can experience a step change of input source or i.e., irradiation, during the period when sunlight is obscured by the Earth or the Moon. This step change of input source can happen right at the time when the sky explorer either enters or leaves the shadow. Second, specific system operation modes, namely the frequent load step between nominal and short circuit [14], [21]–[28] and the load step between nominal and open circuit, are usually adopted in non-terrestrial applications. These modes demand for much faster dynamic responses than those in terrestrial applications. The circuit configuration of these two operation modes (charging modes) are illustrated in Fig. 7 and Fig. 8. In these figures, C_S is the source capacitance, S is a switch, and D_1 is a blocking diode to prevent the load or battery to be shorted when S is turned ON. A battery is the essential source of energy for sky explorers during night time when sunlight is absent. In the load step between nominal and short circuit, the circuit is switching between the short circuit point to the operating point determined by the load applied. In the load step between nominal and open circuit, namely the series switching regulation, a load step is performed between the open circuit condition and the nominal load. The switching

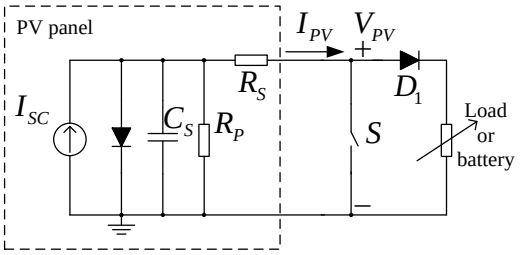


Fig. 7. Circuit configuration of a load step between nominal and short circuit.

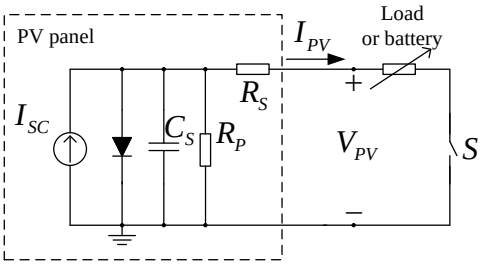


Fig. 8. Circuit configuration of a load step between nominal and open circuit.

frequency of switch S in these tests is, for example, typically 20 kHz such as discussed in [14], but it can be increased to hundreds of kHz. Under these operation modes, the dynamic behavior of the PV panel is significantly important. An ideal PV panel without any capacitance will react immediately without any delay; the transition from one operating point to the other is instantaneous. With the effect of the source capacitor, a practical PV panel under these conditions will react within tens of microseconds, which has been proven in (5).

Because test conditions in terrestrial applications are less extreme compared to those in non-terrestrial applications, a PV emulator designed for terrestrial applications might not be fast enough for testing of non-terrestrial applications. Let us review the performance of existing PV emulators in the next sub-section.

C. Dynamic Performance of Existing PV Emulators

Researchers have proposed different NSEs. They can be classified into the three following categories. The first category is voltage-controlled approach. This is where the power circuit is a voltage-controlled amplifier. The output current is sensed and fed to a reference generator. The reference generator produces a reference output-voltage signal for the power circuit to amplify [1], [29]–[37].

The second category is current-controlled approach, where the power circuit is a current-controlled amplifier. The output voltage is sensed and fed to a reference generator. The reference generator produces a reference output-current signal for the power circuit to amplify [38], [39].

The third category is when both a current controlled and a voltage controlled power circuit are used [40]. In [40], a model-based NSE was developed. The authors used two separate power sources: a controllable linear voltage regulator and a controllable linear current regulator. The voltage regulator is active when the operating points are along the MPP to the open circuit point of the current-voltage (I-V) curve. In a complementary fashion, the current regulator is active when the operating points are along the MPP to the short circuit point. For hot-swapping operation (i.e, continuous transition from using one active power source to the other) when the operating points are close to the MPP, the two power sources are connected with two parallel diodes in order to block the reverse current that may flow from one power source to the other.

In all these three categories, the reference generator can be realized by either an analog or digital circuit. An analog circuit can be based on diode or transistor *p-n* junction [1], [30], [31], or real photo diode illuminated by external light source [29], [32], [33]. A digital circuit can have a core of either a look-up table containing information of I-V curve or a mathematical program that calculates and interpolates the output reference based on its inputs [40]–[42].

Table I summarizes the characteristics of the existing NSEs in terms of their dynamic performance to a load step, the availability of a load step between nominal and short circuit, a load step between nominal and open circuit and an input source step change.

D. Open Challenges

Despite the abundant availability of different existing NSEs, none of them qualifies for non-terrestrial applications. First, all of the important tests namely the load step between nominal and short circuit test, the load step between nominal and open circuit test, and the step change of the input source such as wind, fuel, or irradiation are missing. Most importantly, the existing NSEs are not sufficiently fast to closely resemble real PV arrays. As mentioned in Section I-B, a worst settling time of tens of microseconds is expected under a load step. However, as Table I has shown, the fastest among the existing NSEs needs 3.2 ms [39] to settle, which is a factor of several hundred times slower than the desired tens-of-microsecond response. It can be said that there is an enormous gap from the dynamic performance of existing PV emulators to that of real PV panels under extreme conditions.

E. Scope of This Paper

This paper seeks to address the aforementioned discrepancies in the research about NSEs. The design goal is to achieve a very high dynamic performance NSE that best resembles real PV panels under extreme test conditions. The transient response goal is 10 μs for the load switching operations as well as for the step change of input source. The proposed system, which consists of a non-isolated synchronous buck converter with a fourth order output filter and an analog PV array small signal generator (SSG) circuit, is investigated both theoretically and experimentally. The power rating of the proposed prototype is 200 W. The maximum output power can be changed by adjusting the parallel resistor and the short circuit current reference in the SSG. The experimental results show the proposed NSE can achieve a 10 μs transient

TABLE I
SPECIFICATIONS AND CHARACTERISTICS OF EXISTING PV EMULATORS

Reference(s)	Step change of load settling time	Load step nom. to open	Load step nom. to short	Step change of input source	Power circuit
Koran 2010 [38]	3.8 ms (Fig. 17 of [38])	No	No	No	buck with LCLC filter
Kim 2013 [40]	100 ms (Fig. 15 of [40])	No	No	No	linear voltage & current regulators
Chang 2013 [35]	6 ms (Fig. 12 of [35])	No	No	No	LCLC resonant dc-dc converter
Koran 2014 [39]	3.2 ms (Fig. 15 of [39])	No	No	No	ac-dc three phase rectifier
Gadelovits 2014 [37]	8 ms (Fig. 15 of [37])	No	No	No	commercial power supply
Chang 2014 [36]	6 ms (Fig. 14 of [36])	No	No	No	LCLC resonant dc-dc converter
[1], [29]–[34]	Not found	No	No	No	linear power stage

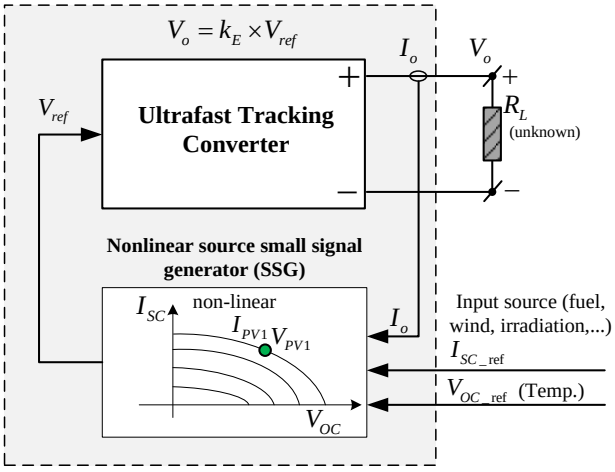


Fig. 9. The proposed system configuration.

response with different test conditions. Moreover, the known prior works are at least 320 times slower, such as ([39], 3.2 ms), ([38], 3.6 ms), ([35], [36], 6 ms), ([37], 8 ms), and ([40], 100 ms). Compared to those works, the proposed converter is much faster as well as closer in resembling a real PV panel's electrical characteristic. It also offers a big advantage in the MPP tracking performance because MPP tracking algorithms would be possibly made faster without compromising the dynamic of the proposed NSE if it were used. From a broader perspective, together with its state-of-the-art dynamic performance, the proposed emulator with proper adjustment will also be able to emulate any slower non-linear sources such as fuel cell and battery, or PV arrays working in terrestrial applications that focus on MPP tracking.

The structure of this paper is as follows. Section I is dedicated to the introduction. Following that, Section II will discuss the proposed NSE, its control approach and circuitry. Section III will present the experimental results. Section IV will be a summary and conclusion of the work.

II. PROPOSED NSE

A. Proposed System Schematic

The proposed system configuration is shown in Fig. 9. The system consists of a voltage-controlled ultrafast tracking converter (VCTC) and a PV array small signal generator (SSG). The proposed system falls into the first category mentioned in Section I-C. In the proposed NSE, the output of the VCTC represents the output of the emulated PV array. The output current is sensed and fed to the SSG. Inside the SSG, the short circuit current and the open circuit voltage can be adjusted. The SSG generates the voltage reference for the ultrafast tracking converter. In this figure, k_E is the dc gain of the VCTC.

In relation to the system configuration shown in Fig. 9, the detailed schematic of the proposed NSE is shown in Fig. 10. In this circuit, the steady-state operation and the gradient of the current-voltage (I-V) curve is determined by three parameters. The short circuit current is determined by the value of I_{SC}; in this prototype, I_{SC} is converted to a voltage signal, $V_{I_{SC}}$, with (1 V/1 A) conversion. Therefore, I_{SC} can be externally programmed by applying a voltage signal $V_{I_{SC}}$ corresponding to it. The parallel resistor, which determines the gradient (or the slope) of the I-V curve around the constant current region, is represented by R_P. The open circuit voltage is controlled by k_E, k_V and R_I. Changing one among these three variables will change the open circuit voltage of the proposed NSE.

The output current I_o is sensed by a precision current sensed resistor of 0.1 Ω in series with the output load R_L. The voltage drop across the sensed resistor is scaled by a factor of 10 to attain a conversion of 1 V/1 A. The output voltage, V_o, and the voltage across capacitor, V_{C_1}, are taken directly to the controller consisting of operational amplifier OA1 and their feedback impedances without any buffering or pre-scaling circuits.

The SSG in the bottom of Fig. 10 consists of summation circuits, a voltage to current (V2I) converter, and a diode circuit. The V2I consists of pnp transistors and operational amplifier OA2. V_{CC} is the 12 V control supply for all the operational and differential amplifiers. The negative control supply, $-V_{CC} = -12$ V, is applied to the cathode of diode D in order to ensure that the V2I converter can operate properly.

As can be seen from the five-parameter model shown in Fig. 4, the current flows through the diode is equal to the difference between the short circuit current I_{SC} and the output current I_o. Using the proposed SSG circuit shown in Fig. 10, the voltage signal that is the difference between I_{SC} and I_o (in volt), is converted to current I_D (in ampere) by:

$$I_D = \frac{V_{I_{SC}} - V_{I_o}}{R_I} \text{ (A)}. \quad (6)$$

Thus, the voltage-drop across diode D and R_P will be the signal level NSE output voltage. A single differential amplifier circuit takes the voltage across D by a summation function denoted by *Sum2* and scales it with a positive gain k_V. Notice the polarity of the summation function *Sum2* in Fig. 10. The resulting voltage, $-V_{ref}$, will be the inverted reference voltage for the VCTC.

The reason for the reference voltage fed to OA1 to be its inverted signal is because it is connected to the inverting input of OA1, which will be then inverted in polarity once again at OA1's output. At the same time, the output voltage V_o and the voltage across the first output filter capacitor V_{C_1} are fed directly to the inverting input of OA1 through their feedback impedance consisting of (R_{d2}, C_{d2}) and (R_{d1}, C_{d1}), respectively. Doing so, the original reference voltage signal will appear at the output of OA1, while the feedback signals will appear with their inverted polarity. The conditioning gains for the feedback signals are primarily determined by the ratios of feedback resistors to R_f, which are (R_{d2}/R_f) for V_o and (R_{d1}/R_f) for V_{C_1}. All of these can be explained further in the modeling of the control system that will be presented later in the next subsection.

It must be noted, that the output voltage of a nonlinear source such as a battery source, a PV panel, or a fuel cell system is usually ripple-free; therefore, the output of a high performance NSE should produce a ripple that is as low as possible. For this reason, a fourth order output filter is utilized at the output of the tracking converter instead of a second order output filter because of its possible higher attenuation, given that the same switching frequency is used. The output filter transfer function, which is from the pulse power signal, V_{pwm}, to the output voltage, V_o, is approximated at high frequency by:

$$G_{FLT}(s)_{(s \gg max(j\omega_1, j\omega_2))} = \frac{V_o(s)}{V_{pwm}(s)}_{(s \gg max(j\omega_1, j\omega_2))} \approx \frac{1}{s^4 L_1 L_2 C_1 C_2} = \frac{\omega_1^2 \omega_2^2}{s^4}, \quad (7)$$

where $\omega_1 = \frac{1}{\sqrt{L_1 C_1}}$ and $\omega_2 = \frac{1}{\sqrt{L_2 C_2}}$ are the natural frequency of each filter stage.

At the switching frequency ω_{sw} (rad/s), the magnitude of the output filter is:

$$|G_{FLT}(j\omega_{sw})| \approx \frac{\omega_1^2 \omega_2^2}{\omega_{sw}^4}. \quad (8)$$

With the filter value provided in Table II and with a switching frequency of 1 MHz, from (8), the fundamental harmonic at the output of the tracking converter will have a magnitude of approximately 35 mV peak to peak.

It needs to be paid attention to, that a hysteresis self-oscillating modulated system as in this case suffers from a variable switching frequency. The switching frequency profile varies along a parabolic curve with regard to the change of duty cycle, where its maximum is at the duty cycle of 0.5 and it reduces quickly when the duty cycle is moving towards either zero or unity [43]–[46]. As (8) has shown, if the switching frequency becomes lower, the output ripple will become higher, which is not desirable. It is suggested that the switching frequency be kept constant regardless of the duty cycle so that a small ripple is always achieved. One of the approaches is to adjust the hysteresis threshold dynamically in a closed loop, such as in [43], [45]. In that approach, the pulse width modulation (PWM) signal frequency is converted to a voltage signal by means of a frequency to voltage converter. The feedback frequency is compared to the reference frequency and the error is processed by a compensator. The output of the compensator adjusts the hysteresis threshold so that the switching frequency converges to the reference frequency. Another approach is to take the output of that compensator and inject it as an absolute gain into the loop that contains the hysteresis modulator, such as in [46]. The practical issue of variable switching frequency inherent in a hysteresis self-oscillating modulated system, however, is not addressed in this paper, which focuses on fast dynamic responses under different load steps and step change of input source. In a similar manner, the design of a power supply that is highly immune to the high *dv/dt* at the output of the NSE can be found in [47]–[50]. Other references relevant to this paper can be found in [54]-[63].

B. Control System Modeling

The block diagram of the control system is shown in Fig. 11. The modeling of the proposed control system is as follows. $G_D(s)$ is the transfer function from the difference between the short circuit current I_{SC} and the output current I_o to the reference voltage V_{ref}:

$$G_D(s) = \frac{k_V Z_D R_P}{R_I(Z_D + R_P)}, \quad (9)$$

where Z_D is the impedance of the diode D used. The transfer function of the proportional-integral-derivative (PID) controller as shown is:

$$G_{PID}(s) = \frac{(R_{pi}C_{pi}s + 1)(R_f C_f s + 1)}{C_{pi} R_f s}. \quad (10)$$

$K_{CMP}(s)$ is the transfer function from the output of the PID controller to the pulse power signal V_{pwm}. A detail treatment of $K_{CMP}(s)$ can be found in, for example, ([51], page 2-4). Works [45], [52] approximated $K_{CMP}(s)$ to be an infinite gain and achieved reasonable results. For simplicity, in this work, K_{CMP} is simplified to be a dc gain which is:

$$K_{CMP}(s) = \frac{V_{pwm}(s)}{V_{carrier}(s)} \approx \frac{V_{DC}}{\varepsilon} = \frac{V_{DC} R_{h2}}{V_{CMP} R_{h1}}, \quad (11)$$

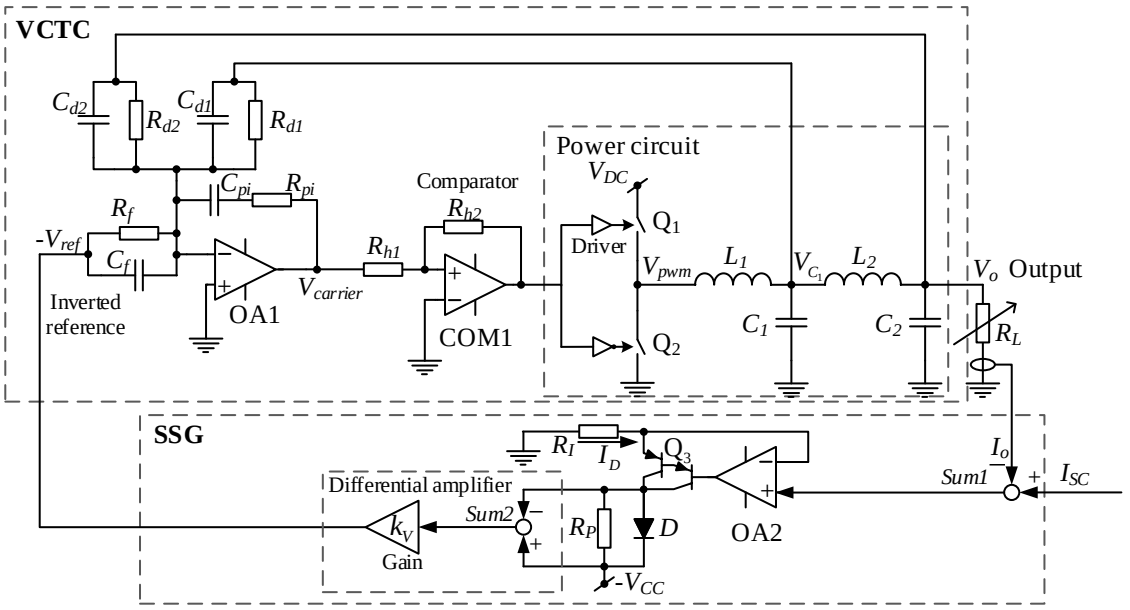


Fig. 10. The schematic of the proposed nonlinear source emulator.

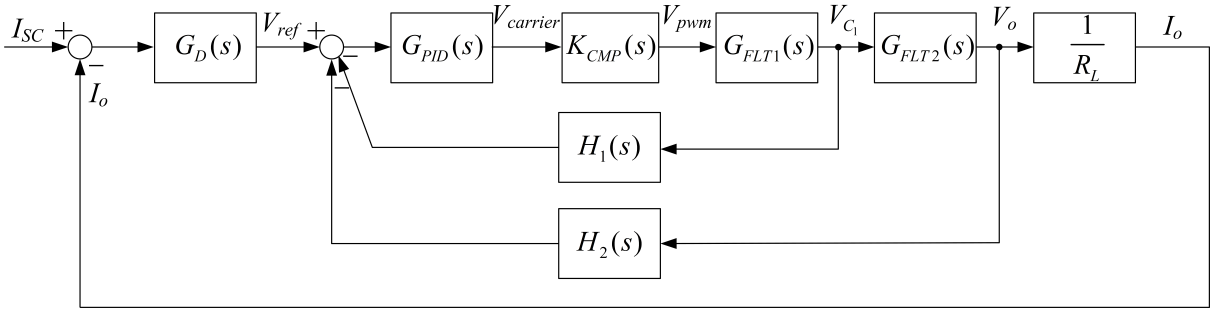


Fig. 11. The block diagram of the control system.

where $\varepsilon = \frac{V_{CMP}R_{h1}}{R_{h2}}$ is the hysteresis threshold, V_{CMP} is the output of the comparator COM1.

$G_{FLT1}(s)$ is the transfer function from V_{pwm} to V_{C_1}, which is (by [45]):

$$G_{FLT1}(s) = \frac{V_{C_1}(s)}{V_{pwm}(s)} = \frac{s^2L_2C_2 + sL_2/R_L + 1}{den(s)}, \quad (12)$$

where the denominator, $den(s)$, is equal to:

$$den(s) = s^4L_1L_2C_1C_2 + s^3L_1L_2C_1/R_L + s^2(L_1C_2 + L_1C_1 + L_2C_2) + s(L_1 + L_2)/R_L + 1. \quad (13)$$

$G_{FLT2}(s)$ is the transfer function from V_{C_1} to V_o, which is:

$$G_{FLT2}(s) = \frac{V_o(s)}{V_{C_1}(s)} = \frac{1}{s^2L_2C_2 + sL_2/R_L + 1}. \quad (14)$$

The most inner feedback transfer function is:

$$H_1(s) = \frac{R_f(R_{d1}C_{d1}s + 1)}{R_{d1}(R_fC_fs + 1)}. \quad (15)$$

Likewise, the output-voltage feedback transfer function is:

$$H_2(s) = \frac{R_f(R_{d2}C_{d2}s + 1)}{R_{d2}(R_fC_fs + 1)}. \quad (16)$$

The most inner loop closed loop transfer function is:

$$G_{IN-CL}(s) = \frac{V_{C_1}(s)}{V_{ref}(s) - V_o(s)H_2(s)} = \frac{G_{PID}(s)K_{CMP}(s)G_{FLT1}(s)}{1 + G_{PID}(s)K_{CMP}(s)G_{FLT1}(s)H_1(s)}. \quad (17)$$

Since $K_{CMP}(s)$ is a very high gain, $G_{IN-CL}(s)$ can be approximated to be:

$$G_{IN-CL}(s) \approx \frac{1}{H_1(s)}. \quad (18)$$

The transfer function from the reference voltage to the output voltage is then:

$$G_V(s) = \frac{V_o(s)}{V_{ref}(s)} = \frac{G_{IN-CL}(s)G_{FLT2}(s)}{1 + G_{IN-CL}(s)G_{FLT2}(s)H_2(s)} \quad (19)$$

$$\approx \frac{G_{FLT2}(s)}{H_1(s) + G_{FLT2}(s)H_2(s)}. \quad (20)$$

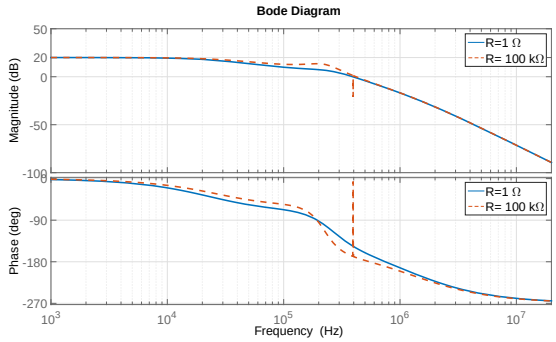


Fig. 12. Bode plot of the closed voltage loop $G_V(s)$ at different loads.

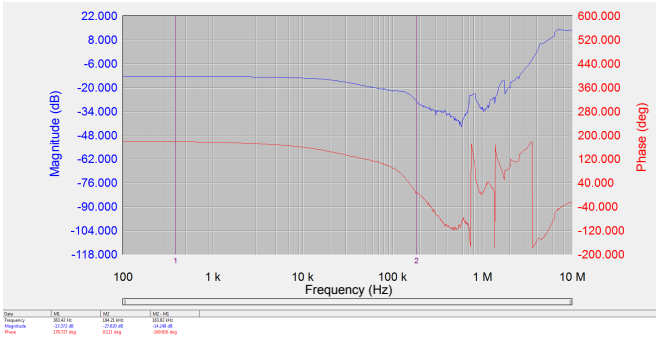


Fig. 13. Measured Bode plot of the transfer function from $V_{ref}(s)$ to $I_o(s)$ at 47 Ω load.

A Bode plot of $G_V(s)$ based on (19) and the parameters in Table II is shown in Fig. 12 for different loads.

Fig. 13 shows the transfer function from $V_{ref}(s)$ to $I_o(s)$ at 47 Ω load measured with the Bode 100 Analyzer. This transfer function is equal to the closed loop transfer function from $V_{ref}(s)$ to $V_o(s)$ divided by a load of 47 Ω, or 33.4 dBΩ. Therefore, the dc gain of the measurement (the blue curve) is 20dB − 33.4dB = −13.4dB. The phase shown in the red curve is measured in closed loop, so it is equal to the phase of the transfer function from $V_{ref}(s)$ to $V_o(s)$ plus 180 °. It can be seen the shape and value of the gain and phase correspond well with those in the model of Fig. 12, except for the high frequency region where sampling effects at the switching frequency and above occur.

With the circuit schematic shown in Fig. 10, the amplification factor k_E of the closed loop tracking converter shown in Fig. 9 will have the following formula:

$$k_E = G_V(0) = \frac{R_{d1}R_{d2}}{R_f(R_{d1}+R_{d2})}. \quad (21)$$

From the resistance values in Table II, k_E is equal to 10. Thus, one volt of the reference voltage V_{ref} will produce ten volts of the output voltage V_o.

III. Experimental Results

The experimental studies have examined the proposed NSE under three typical operating conditions usually faced in non-terrestrial applications. They are the steady-state response along the static I-V curve, the series switching regulator tests, and the step change of input source. In addition, the fourth test is also added, that is a *fictitious* step change of temperature. The fourth test is fictitious because a step change of temperature is physically unrealizable because of the thermal inertia of the PV material. After a sudden change of input source, a PV panel will usually take approximately 30 minutes to reach its steady-state temperature [53]. Although a step change of temperature is unlikely, the test will still be carried out here in this work in order to verify the dynamic capability of the proposed NSE.

TABLE II
Parameters of the Tracking Converter and its Control

L_1	3.3 μH	C_f	1 nF
L_2	3.3 μH	R_{d1}	20 kΩ
C_1	100 nF	C_{d1}	47 pF
C_2	1360 nF	R_{d2}	20 kΩ
V_{DC}	60 V	C_{d2}	470 pF
R_{h1}	6.2 kΩ	R_{pi}	1 kΩ
R_{h2}	51 kΩ	C_{pi}	470 pF
R_f	1 kΩ	V_{CMP}	5 V
k_E	10		

The proposed circuit, unfortunately, suffers from instability at short circuit current. According to [40], this is an intrinsic characteristic of the voltage-control approach. Also according to [40], the current control approach does not have similar problem in the short circuit region, but it suffers from poor controllability and stability near the open circuit region.

The instability of the proposed NSE at operating points close to the short circuit can be explained as follows. Near the short circuit region of the I-V curve, the load impedance R_L is small in Ohmic value, making the gain from V_o to I_o become large compared to that in other region. In addition, the output current is approaching I_{SC}, which will make I_D approach zero. This small current makes the impedance of diode D approach infinitive according to the diode I-V curve. This makes $G_D(s)$ becomes very large. The open-loop gain that consists of $G_D(s), G_V(s)$, and $\frac{1}{R_L}$ becomes also very large. Its cross-over frequency will move towards higher frequency, where the phase margin becomes negative (see Fig. 12), which in turn causes the system instability.

The load step between nominal and short circuit problem of voltage-controlled NSE will not be addressed in this paper; it may the treated in a separate future work.

A photo of the prototype can be found in Fig. 14. The prototype has a dimension of 10 cm×10 cm. The upper part is the power circuit, which is the synchronous buck converter with two stage LC output filter plus a heat sink. The lower part contains all the feedback and control circuitry.

A. Steady-State Response

Figs. 15 and 16 show the steady-state current-voltage (I-V) and power-voltage (P-V) curves generated by the prototype with the set up in Table III. The short circuit current is programmed to be 5 A by inputting a voltage $V_{I_{SC}}$ of 5 V. When the load is open, there will be no output current and therefore, V_{I_o} is equal to zero. According to (6), a forward current of 0.33 A will flow through diode D. This develops

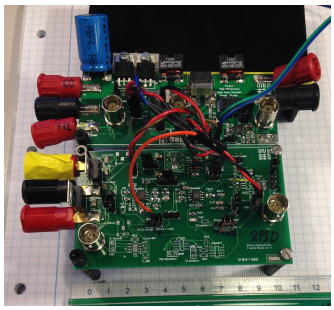


Fig. 14. A photo of the prototype.

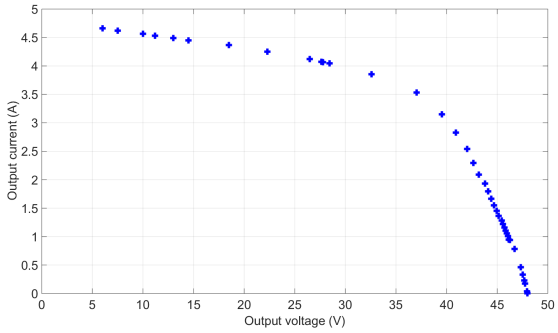


Fig. 15. The static current-voltage (I-V) curve generated by the proposed NSE.

a diode forward voltage drop of approximately 0.96 V. With the gain factor k_V of the differential amplifier equal to 5, this gives a voltage reference V_{ref} of approximately 4.8 V. This results in an open circuit voltage of 48 V because k_E is equal to 10 by design.

As can be seen, the output voltage and current resemble the output of a PV panel. The MPP with this set up is 131 W at a load impedance of approximately 10 Ω.

B. Series Switching Regulation

Fig. 17 shows the transient responses of the proposed NSE under a series-type switching regulation. The load is switching between two values: open circuit (where the load is infinitive) and a fixed load. The switching frequency of the load is about 1 kHz. As can be seen, the output voltage and current finish each transient within 10 μs. It is interesting to observe the experimental I-V curve of this test recorded directly from the oscilloscope used in the tests, which can be referred to Fig. 18a. Meanwhile, Fig. 18b explains the process of Fig. 18a, which will be as follows. The NSE is switching between

TABLE III
PARAMETERS USED TO GENERATE STATIC I-V CURVE

Parameter	Value
I_{SC}	5 A
R_P	10 Ω
R_I	15 Ω
k_V	5
V_{OC}	48 V

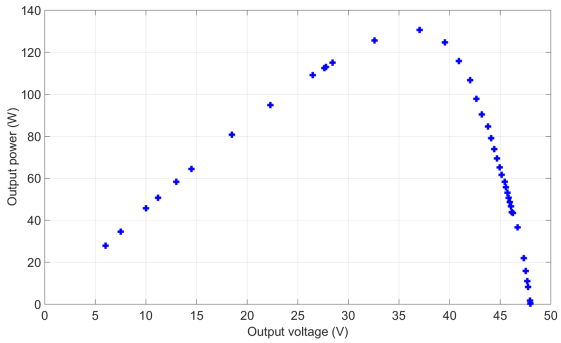


Fig. 16. The static power-voltage (P-V) curve generated by the proposed NSE.

denoted operating points A and B of Fig. 18b. Right after the fixed load is inserted to the output of NSE, the circuit immediately moves from operating point A to interim point A1. During this period, the voltage does not change yet due to its disturbance rejection capability, while the new current value will be the result of the voltage at operating point A divided by the fixed load. After that, the regulation of the NSE makes the circuit move from A1 to operating point B, and the whole process from A to B takes only 10 μs (see Fig. 17c). From that moment, the circuit settles at B until the load experiences a new step change. Likewise, when the load is switched from the fixed load to open circuit, which enforces a transient from operating point B to A, the operating point will first and immediately move from B to interim point B1. Following that, it will move from B1 to A and settle at A. The whole transition from B to A also takes only 10 μs, which can be verified from Fig. 17b.

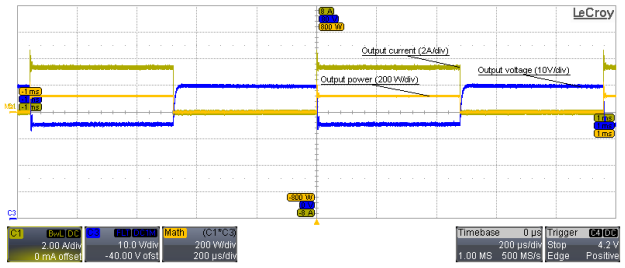
The two arrows in Fig. 18a are originated from two cursors of the oscilloscope. They show the location of the operating point (A and B) in Fig. 18, but they are not visible from Fig. 17.

C. Step Change of Input Source

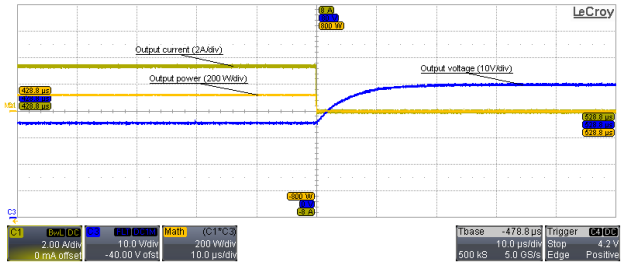
The results of the step change of input source are shown in Figs. 19 and 20. In Fig. 19, channel 2 (red color) is the short circuit current I_{SC}. The input source change causes a change of short circuit current from 2 to 5 A and *vice versa*. From Figs. 19b and 19c, the circuit only takes 10 μs to complete the transition. The experimental I-V curve is shown in Fig. 20a and its behavior is explained in Fig. 20b. A reduction of input source level from 5 to 2 A short circuit current will make the NSE move from point A to B, and an increase of input source in the other direction will make the NSE move from point B to A. Each transition takes only 10 μs.

D. Dynamic Change of Temperature

As discussed in Section II-A, the open circuit voltage is determined by k_E, k_V, and R_I. Furthermore, the open circuit voltage is mainly determined by the temperature. Therefore, changing the open circuit voltage by means of adjusting one



(a)



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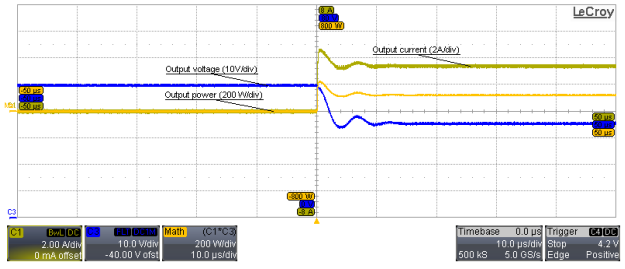
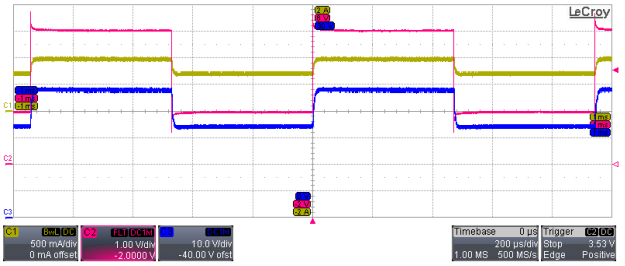
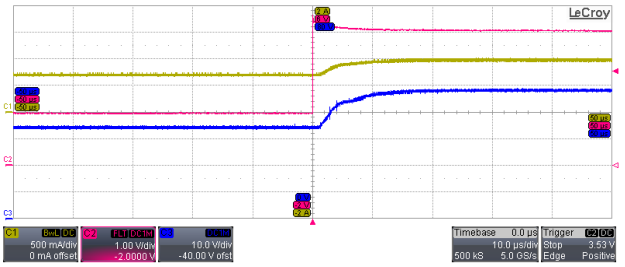


(c)

Fig. 17. Series load step test (a) switching transient between a nominal load and open circuit (b) partial zoom of the circuit transients from nominal load to open circuit (c) partial zoom of the circuit transients from open circuit to nominal load. Channel 1 (olive color): output current, 2 A/div. Channel 3 (blue color): output voltage, 10 V/div. Channel Math (C1*C3) (orange color): output power, 200 W/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.



(a)



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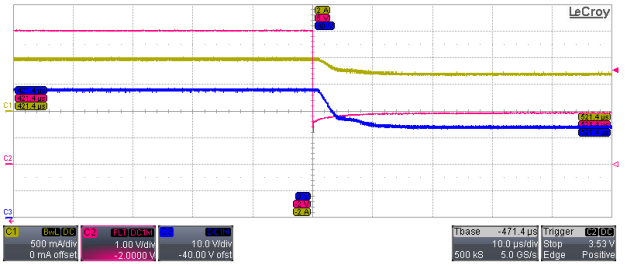
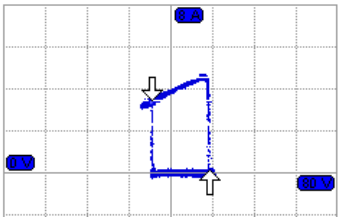
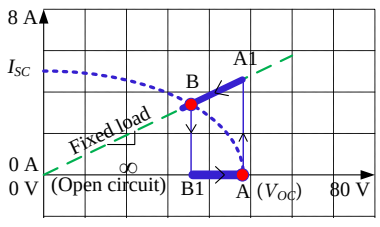


(c)

Fig. 19. Emulation of input source step change (a) switching transient between two input source levels (b) partial zoom of the transients from a low to high input source level (c) partial zoom of the transients from a high to low input source level. Channel 1 (olive color): output current, 2 A/div. Channel 3 (blue color): output voltage, 10 V/div. Channel 2 (red color): input source level, 1 A/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.

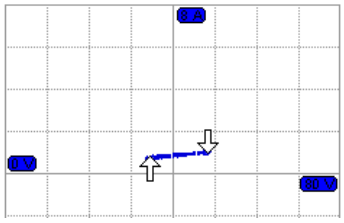


(a)

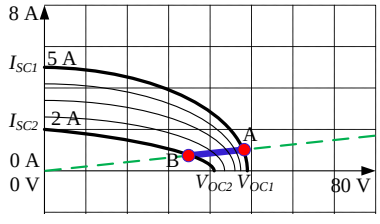


(b)

Fig. 18. Series test. (a) Experimental I-V curve and (b) its analytical waveform.



(a)

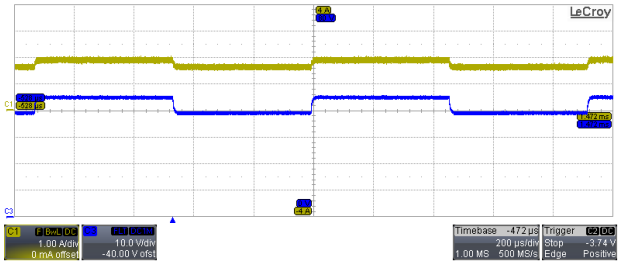


(b)

Fig. 20. Step change of input source. (a) Experimental I-V curve and (b) its analytical waveform.

of the three parameters k_E, k_V, and R_I will give the same effect as changing temperature.

The fictitious step change of temperature can be simulated by performing a step change between different values of R_I. To demonstrate this, the value of R_I is switched back and forward between 15 and 30 Ω. The results are shown in Figs. 21 and 22. The short circuit current is fixed at 5 A. When changing the temperature, the short circuit current does not change, but the profile of I-V curve changes as shown in Fig. 22b. As can be seen from these results, under a step change of temperature, the proposed NSE only takes about 10 μs to complete a transition.



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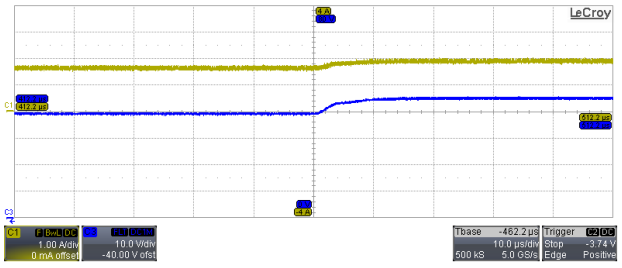

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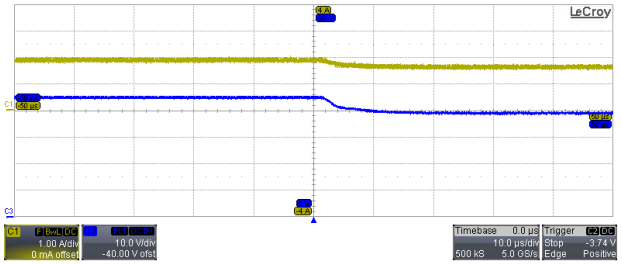
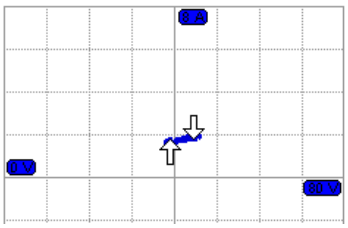


(c)

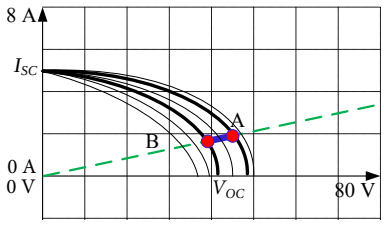
Fig. 21. Emulation of fictitious temperature step change (a) switching transient between two temperature levels (b) partial zoom of the transients from a low to high temperature level (c) partial zoom of the transients from a high to low temperature level. Channel 1 (olive color): output current, 1 A/div. Channel 3 (blue color): output voltage, 10 V/div. Time scale: 200 μs/div, 10 μs/div, and 10 μs/div, respectively.

IV. Conclusion

This paper has proposed and demonstrated an NSE system with high dynamic performance. The result that has been achieved is a 200-W NSE capable of simulating series-type switching tests and step change of input source tests with the fastest transient response ever reported, 10 μs. This work, therefore, has provided a state-of-the-art solution for simulating different nonlinear sources in non-terrestrial as well as terrestrial applications.



(a)



(b)

Fig. 22. Fictitious temperature step change effect. (a) Experimental I-V curve and (b) its analytical waveform.

The presence of the intrinsic source capacitance in a real PV system determines its transient response under a load step. This quantity should be taken into account in the design of the PV emulator. In addition, the output of a nonlinear source usually does not contain ripple. Therefore, it is desired that the developed NSE's output ripple to be as low as possible. This can be achieved by high order filtering of the NSE. The switching frequency drop that is inherent in a hysteresis self-oscillating controlled system needs to be paid attention because it increases the output voltage ripple.

It must be acknowledged, however, that the proposed method contains several limitations. The first issue is the stability when the NSE operates in the short circuit region. One approach is to design a more robust control structure, which raises open issues for future study. Another approach is to use a dual-mode power circuit that consists of a separate voltage source and a separate current source power circuit. Deactivating the voltage source and activating the current source power circuit when the NSE operates in the short circuit region may solve the problem. The second issue is to solve the load step between nominal and short circuit. Once the stability issue in the short circuit region is solved, this issue may get easier to be tackled.

Finally, for future work, it might be beneficial to realize the nonlinear curve small signal reference generator by means of an advanced digital control unit, such as high-speed FPGA, in order to take into account multiple parameter changes at the same time or to allow for more flexible setting of test conditions.

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REFERENCES

[1] D. Schofield, M. Foster, and D. Stone, "Low-cost solar emulator for evaluation of maximum power point tracking methods," *Electronics Letters*, vol. 47, no. 3, pp. 208–209, February 2011.

[2] C. Park, J. Liu, and P. Chou, "B#: a battery emulator and power-profiling instrument," *Design Test of Computers, IEEE*, vol. 22, no. 2, pp. 150–159, March 2005.

[3] P. Chou, C. Park, J. Park, K. Pham, and J. Liu, "B#: a battery emulator and power profiling instrument," in *Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on*, Aug 2003, pp. 288–293.

[4] O. Konig, S. Jakubek, and G. Prochart, "Model predictive control of a battery emulator for testing of hybrid and electric powertrains," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, Sept 2011, pp. 1–6.

[5] ——, "Battery impedance emulation for hybrid and electric powertrain testing," in *Vehicle Power and Propulsion Conference (VPPC), 2012 IEEE*, Oct 2012, pp. 627–632.

[6] O. Konig, C. Hametner, G. Prochart, and S. Jakubek, "Battery emulation for power-hil using local model networks and robust impedance control," *Industrial Electronics, IEEE Transactions on*, vol. 61, no. 2, pp. 943–955, Feb 2014.

[7] T. Mesbahi, N. Rizoug, P. Bartholomeus, and P. Le Moigne, "Li-ion battery emulator for electric vehicle applications," in *Vehicle Power and Propulsion Conference (VPPC), 2013 IEEE*, Oct 2013, pp. 1–8.

[8] A. Thanheiser, T. Kohler, C. Bertram, and H. Herzog, "Battery emulation considering thermal behavior," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, Sept 2011, pp. 1–5.

[9] J. Correa, F. Farret, J. Gomes, and M. Simoes, "Simulation of fuel-cell stacks using a computer-controlled power rectifier with the purposes of actual high-power injection applications," *Industry Applications, IEEE Transactions on*, vol. 39, no. 4, pp. 1136–1142, July 2003.

[10] M. Ordonez, M. Iqbal, and J. Quaicoe, "Development of a fuel cell simulator based on an experimentally derived model," in *Electrical and Computer Engineering, 2005. Canadian Conference on*, May 2005, pp. 1449–1452.

[11] J.-G. Lim, S.-H. Kim, E.-K. Seo, H.-B. Shin, S.-K. Chung, and H. woo Lee, "Implementation of fuel cell dynamic simulator," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, June 2006, pp. 1–5.

[12] J.-G. Lim and S.-K. Chung, "Implementation of a fuel cell dynamic simulator," *Journal of Power Electronics*, vol. 7, no. 4, pp. 336–342, 2007.

[13] P. Acharya, P. Enjeti, and I. Pitel, "An advanced fuel cell simulator," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 3, 2004, pp. 1554–1558 Vol.3.

[14] R. Kumar, M. Suresh, and J. Nagaraju, "Effect of solar array capacitance on the performance of switching shunt voltage regulator," *Power Electronics, IEEE Transactions on*, vol. 21, no. 2, pp. 543–548, March 2006.

[15] J. Ibirriaga, X. de Mendiluce Pena, A. Opritescu, D. Sera, and R. Teodorescu, "Low-cost, high flexibility i-v curve tracer for photovoltaic modules," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on*, May 2010, pp. 1210–1215.

[16] D. S. H. Chan and J. C. H. Phang, "Analytical methods for the extraction of solar-cell single- and double-diode model parameters from i-v characteristics," *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 286–293, Feb 1987.

[17] K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "A review on the implementation of nonlinear source emulators," in *55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University*, October 2014, pp. 56–62.

[18] C. Honsberg and S. Bowden, "Series resisrance," November 2014. [Online]. Available: http://www.pveducation.org/pvcdrom/solar-cell-operation/series-resistance

[19] T. Esram and P. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *Energy Conversion, IEEE Transactions on*, vol. 22, no. 2, pp. 439–449, June 2007.

[20] G. J. Madden and A. Le, "Solar panel model for design and analysis of power regulation equipment," *Proceedings of the Intersociety Energy Conversion Engineering Conference*, vol. 1, pp. 151–156, 1994.

[21] J. M. Blanes, A. Garrigs, E. Sanchis, and J. A. Carrasco, "Modeling the sequential switching shunt series regulator," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 7–13, 2005.

[22] "Shunt-mode solar/wind charge controller," February 2014. [Online]. Available: http://www.solorb.com/elect/solarcirc/shuntreg1/

[23] A. Patil, B. Cho, and F. Lee, "Design considerations for a solar array switching unit," in *Energy Conversion Engineering Conference, 1990. IECEC-90. Proceedings of the 25th Intersociety*, vol. 1, Aug 1990, pp. 373–379.

[24] B. S. N. U. K. Cho, D. V. P. I. Lee, and S. Univ., *A single PWM section solar array shunt switching unit with an active ripple filter*. American Society of Mechanical Engineers, New York, NY (United States), Dec 1995.

[25] J. M. Blanes, A. Garrigs, E. Sanchis-Kilders, and J. A. Carrasco, "A new sequential switching shunt regulator - digital shunt regulator (s3r-dsr) for solar array regulators," *IEEE International Symposium on Industrial Electronics*, vol. 2, pp. 1064–1069, 2006.

[26] A. Garrigos, J. Blanes, J. Carrasco, and J. Ejea, "Influence of the parasitic solar array capacitance in the sequential switching shunt series regulator," in *Electrotechnical Conference, 2006. MELECON 2006. IEEE Mediterranean*, May 2006, pp. 1198–1201.

[27] K. E. Shum and C. R. Ashley, "A new full shunt switching unit for solar array using coupled-inductor boost converter," *Proceedings of the Intersociety Energy Conversion Engineering Conference*, vol. 1, pp. 617–622 vol.1, 1996.

[28] K. Wu, "Loop gain of a spacecraft switched shunt power system," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 30, no. 4, pp. 1049–1053, 1994.

[29] S. Armstrong, C. K. Lee, and W. Hurley, "Investigation of the harmonic response of a photovoltaic system with a solar emulator," in *Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 8 pp.–P.8.

[30] "Two bipolar transistors form a low-cost solar-array emulator," December 2013. [Online]. Available: http://electronicdesign.com/energy/two-bipolar-transistors-form-low-cost-solar-array-emulator

[31] W. kui, L. Yongdong, R. Jianye, and S. Min, "Design and implementation of a solar array simulator," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on*, Oct 2008, pp. 2633–2636.

[32] H. Nagayoshi, "Characterization of the module/array simulator using i-v magnifier circuit of a pn photo-sensor," in *Photovoltaic Energy Conversion, 2003. Proceedings of 3rd World Conference on*, vol. 2, May 2003, pp. 2023–2026 Vol.2.

[33] ——, "Iv curve simulation by multi-module simulator using iv magnifier circuit," *Solar Energy Materials and Solar Cells*, vol. 82, no. 12, pp. 159 – 167, 2004, {CANCUN} 2003. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0927024804000236

[34] H. Nagayoshi and M. Atesh, "Partial shading effect emulation using multi small scale module simulator units," in *Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE*, Jan 2005, pp. 1710–1713.

[35] C.-H. Chang, E.-C. Chang, and H.-L. Cheng, "A high-efficiency solar array simulator implemented by an llc resonant dc-dc converter," *Power Electronics, IEEE Transactions on*, vol. 28, no. 6, pp. 3039–3046, June 2013.

[36] C. Chang, C. Cheng, and H. Cheng, "Modeling and design of the llc resonant converter used as a solar-array simulator," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, no. 4, pp. 833–841, Dec 2014.

[37] S. Gadelovits, M. Sitbon, and A. Kuperman, "Rapid prototyping of a low-cost solar array simulator using an off-the-shelf dc power supply," *Power Electronics, IEEE Transactions on*, vol. 29, no. 10, pp. 5278–5284, Oct 2014.

[38] A. Koran, K. Sano, R. young Kim, and J.-S. Lai, "Design of a photovoltaic simulator with a novel reference signal generator and two-stage lc output filter," *Power Electronics, IEEE Transactions on*, vol. 25, no. 5, pp. 1331–1338, May 2010.

[39] A. Koran, T. LaBella, and J.-S. Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *Power Electronics, IEEE Transactions on*, vol. 29, no. 3, pp. 1285–1297, March 2014.

[40] Y. Kim, W. Lee, M. Pedram, and N. Chang, "Dual-mode power regulator for photovoltaic module emulation," *Applied Energy*, vol. 101, no. 0, pp. 730 – 739, 2013, sustainable Development of Energy, Water and Environment Systems. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0306261912005375

[41] E. Koutroulis, K. Kalaitzakis, and V. Tzitzilonis, "Development of an fpga-based system for real-time simulation of photovoltaic modules," in *Rapid System Prototyping, 2006. Seventeenth IEEE International Workshop on*, June 2006, pp. 200–208.

[42] Y. Li, T. Lee, F. Peng, and D. Liu, "A hybrid control strategy for photovoltaic simulator," in *Applied Power Electronics Conference and*

Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE, Feb 2009, pp. 899–903.
[43] D. Grant, "Frequency control of hysteretic power converter by adjusting hystersis levels," Feb. 19 2002, uS Patent 6,348,780.
[44] S. Poulsen and M. Andersen, "Hysteresis controller with constant switching frequency," *Consumer Electronics, IEEE Transactions on*, vol. 51, no. 2, pp. 688–693, May 2005.
[45] M. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2387–2398, Sept 2008.
[46] K. Nguyen-Duy, A. Knott, and M. Andersen, "Constant switching frequency self-oscillating controlled class-d amplifiers," *Elektronika ir Elektrotechnika*, vol. 20, no. 6, pp. 84–88, 2014.
[47] K. Nguyen-Duy, L. Petersen, A. Knott, O. Thomsen, and M. Andersen, "Design of a 300-watt isolated power supply with minimized circuit input-to-output parasitic capacitance," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, April 2014, pp. 1–6.
[48] K. Nguyen-Duy, Z. Ouyang, L. Petersen, A. Knott, O. Thomsen, and M. Andersen, "Design of a 300-watt isolated power supply for ultra-fast tracking converters," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2014.
[49] K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. Andersen, "Minimization of the transformer inter-winding parasitic capacitance for modular stacking power supply applications," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, Aug 2014, pp. 1–10.
[50] K. Nguyen-Duy, A. Knott, and M. Andersen, "Loss performance analysis of an isolated power supply for ultrafast tracking converters," in *IEEE International Power Electronics and Application Conference and Exposition (IEEE PEAC'2014)*, November 2014, pp. 1543–1548.
[51] M. C. W. Høyerby and M. A. E. Andersen, "A small-signal model of the hysteretic comparator in linear-carrier self-oscillating switch-mode controllers," in *Nordic Workshop on Power and Industrial Electronics*, 2006.
[52] M. Hoyerby and M. A. E. Andersen, "Optimized envelope tracking power supply for tetra2 base station rf power amplifier," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, Feb 2008, pp. 777–783.
[53] "Mpp solar tracker: the effect of module temperature and insolation," November 2014. [Online]. Available: http://hespv.ca/hesproductspecs/technical-bulletins/fronius/SE_TA_MPP_Solar_Tracker_Effect_Module_Temperature_Insolation_EN_320488_snapshot.pdf
[54] Z. Housheng and Z. Yanlei, "Research on a novel digital photovoltaic array simulator," in *Intelligent Computation Technology and Automation (ICICTA), 2010 International Conference on*, vol. 2, May 2010, pp. 1077–1080.
[55] R. Kumar, M. Suresh, and J. Nagaraju, "Measurement of ac parameters of gallium arsenide (gaas/ge) solar cell by impedance spectroscopy," *Electron Devices, IEEE Transactions on*, vol. 48, no. 9, pp. 2177–2179, Sep 2001.
[56] R. A. Kumar, M. Suresh, and J. Nagaraju, "Measurement and comparison of {AC} parameters of silicon (bsr and bsfr) and gallium arsenide (gaas/ge) solar cells used in space applications," *Solar Energy Materials and Solar Cells*, vol. 60, no. 2, pp. 155 – 166, 2000. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S092702489900080X
[57] K.-D. Rasch and K. Roy, "Shunt and blocking diodes for protection of space solar arrays." *Conference Record of the IEEE Photovoltaic Specialists Conference*, pp. 550–553, 1981.
[58] N. N. Goryashin and A. S. Sidorov, "Solar array regulator based on buck converter with sequential switched sections," *International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices, EDM*, pp. 364–368, 2013.
[59] M. Mira, A. Knott, O. Thomsen, and M. Andersen, "Boost converter with combined control loop for a stand-alone photovoltaic battery charge system," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, June 2013, pp. 1–8.
[60] M. Hoyerby and M. A. E. Andersen, "Teds base-station power amplifier using low-noise envelope tracking power supply," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 7, pp. 1687–1693, July 2009.
[61] M. Hoyerby and M. Andersen, "Carrier distortion in hysteretic self-oscillating class-d audio power amplifiers: Analysis and optimization," *Power Electronics, IEEE Transactions on*, vol. 24, no. 3, pp. 714–729, March 2009.
[62] M. Villalva, J. Gazoli, and E. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *Power Electronics, IEEE Transactions on*, vol. 24, no. 5, pp. 1198–1208, May 2009.
[63] L. Nousiainen, J. Puukko, A. Maki, T. Messo, J. Huusari, J. Jokipii, J. Viinamaki, D. Lobera, S. Valkealahti, and T. Suntio, "Photovoltaic generator as an input source for power electronic converters," *Power Electronics, IEEE Transactions on*, vol. 28, no. 6, pp. 3028–3038, June 2013.

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